WEST Search History

DATE: Monday, November 17, 2003

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	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L14	((pll) or (phase near5 frequency) near4 detect$3) same (cmos near3 invert$3) same (charge near3 pump$3)	2	L14
L13	l5 and (external$23 near2 power near2 supply$3) and l3	1	L13
L12	L11 and l9 and l8	16	L12
L11	bocure.xa. or bocure.xp.	1043	L11
L10	L9 and l7 and l8	72	L10
L9	(375/356)!.CCLS. or 375/371.ccls. or 375/354.ccls.	5188	L9
L8	(clock near3 distribut$3)	6955	L8
L7	bocure.xa. nor bocure.xp.	353518	L7
L6	L5 and l3	39	L6
L5	(clock near3 distribut$3) and ((pll) or (phase near lock$3 near loop$)) and ((phase near5 frequency) near4 detect$3) and (power near supply$3)	77	L5
L4	L3 and l2	3	L4
L3	@ad<=19970627	15284040	L3
L2	(clock near3 distribut$3) same ((pll) or (phase near5 frequency) near4 detect$3) same (power near supply$3)	18	L2
L1	(clock near3 distribut$3) same ((pll) or (phase adj2 lock$23 adj3 loop)) same (power near supply$3)	19	L1

END OF SEARCH HISTORY

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L18: Entry 7 of 19 File: USPT Dec 12, 1995

DOCUMENT-IDENTIFIER: US 5475718 A
TITLE: Digital phase-locked loop

Application Filing Date (1):
19940207

Brief Summary Text (10):
In digital communication systems it is necessary to synchronize the clock of a received signal with that of the transmitted signal. Normally, the clock of the transmitted signal is derived from the data signal. The derived clock representing the output signal of an oscillator in the receiving system is to correspond as regards frequency and phase to the clock of the transmitted signal which is to be considered the reference signal. For synchronizing the pulse-shaped oscillator signal with the pulse-shaped reference signal, a digital phase-locked loop is used. The digital phase-locked loop comprises a digital controller which can be easily realised with a signal processor. A suitable controller for the present use is, for example, a PI controller. This controller comprises a proportional element and an integral element. Furthermore, a controllable oscillator is included. The frequency of this oscillator is adjusted by means of the digital output signals of the controller. A first input of a phase detector, whose second input is arranged for receiving a pulse-shaped reference signal, is coupled to the output of the oscillator. The output signal of the phase detector determines the phase difference between reference and oscillator signal. The output of the phase detector is coupled to the input of the digital controller.

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L13: Entry 1 of 1 File: USPT Jul 21, 1998

DOCUMENT-IDENTIFIER: US 5783956 A
TITLE: Semiconductor device realizing internal operation factor corresponding to an external operational factor stably regardless of fluctuation of the external operational factor

Abstract Text (1):
A semiconductor memory device includes a difference adjusting circuit for detecting difference in at least one of phase and frequency between an external clock signal and an internal clock signal, for outputting a control potential for reducing the difference, and a current control circuit for adjusting driving current of an internal clock signal generating circuit in accordance with an output potential from the difference adjusting circuit. The current control circuit includes a current change restricting circuit for making smaller an amount of change of current in the clock signal generating circuit with respect to the change in the output potential from the difference adjusting circuit. An internal power supply voltage obtained by lowering internally the external power supply voltage is applied to the clock signal generating circuit. Further, when supply of the external clock signal is stopped, the output potential from the difference adjusting circuit is held. The internal power supply potential generating circuit further includes a current control circuit for adjusting an amount of current for supplying the internal power supply potential in accordance with the difference between an internal power supply potential and a prescribed potential level.

Application Filing Date (1):
19960131

Brief Summary Text (3):
The present invention relates to a semiconductor device for generating an internal operational factor corresponding to an external operational factor such as a power supply voltage or a clock signal. More specifically, the present invention relates to a semiconductor device including a phase locked loop (PLL) circuit or a delay locked loop (DLL) circuit or a ring oscillator for generating an internal clock signal and/or a semiconductor device including a down converter for generating an internal power supply potential by down-converting level of an externally applied power supply potential.

Brief Summary Text (5):
A PLL circuit has been known as a circuit for generating an internal signal which is in phase/frequency synchronization with an externally applied signal. The PLL circuit is used for reproducing color subcarrier for synchronous detection of a color burst signal in an integrated circuit for reproducing an ATC (Automatic Control) type color subcarrier, for improving stability of color reproduction in a color television. It is also used in the field of wire communication for synchronizing a clock output from a highly stable oscillator arranged in one station with a reference clock received from a high level station so as to distribute stable clock to various communication devices in the station.

Brief Summary Text (6):
FIG. 1 shows a schematic structure of a conventional PLL. Referring to FIG. 1, the PLL circuit includes a phase comparator circuit 2 receiving an internal clock intCLK and an external clock extCLK for outputting control signals UP and/DOWN corresponding to frequency and phase deviation between the internal clock intCLK and the external clock extCLK; a charge pump circuit 3 for adjusting potential level of its output node 3a in accordance with the control signals UP and/DOWN from phase comparator circuit 2; a loop filter 4 for filtering the output signal (potential)

from output node 3a of charge pump circuit 3; a current adjusting potential output circuit 5 receiving the output potential VP from loop filter 4 for outputting an output potential VN corresponding to the output potential VP; and a ring oscillator having its oscillation frequency controlled in accordance with the output potential VP from loop filter 4 and the potential VN from current adjusting potential output circuit 5. The internal clock intCLK is output from ring oscillator 6.

Brief Summary Text (7):
Phase comparator 2 has a structure of a phase frequency comparator (PFC) and it sets the control signal UP at an L (low) level when the frequency of the internal clock intCLK is larger than the frequency of the external clock extCLK or when the phase of the internal clock intCLK is in advance of the phase of the external clock extCLK, and it sets the control signal UP at an H (high) level when the frequency of the internal clock intCLK is smaller than the frequency of the external clock extCLK or when the phase of the internal clock intCLK is lagged from that of the external clock extCLK. The control signal /DOWN from the phase comparator circuit 2 is set to the L level when the frequency of the internal clock intCLK is larger than the frequency of external clock extCLK or the phase of internal clock intCLK is in advance of the phase of the external clock extCLK, and it is set to the H level when the frequency of the internal clock intCLK is smaller than the frequency of the external clock extCLK or when the phase of the internal clock intCLK is lagged from the phase of the external clock extCLK. The phase comparator circuit 2 operates as a frequency error detector automatically when unlocked, and operates as a phase difference detector in a capture range.

Brief Summary Text (8):
Charge pump circuit 3 includes a constant current circuit 3c connected between a power supply node 1a to which the power supply potential VCC is applied and a node 3b, for supplying a constant current to node 3b; a p channel MOS (insulated gate type field effect) transistor 3d connected between node 3b and an output node 2a and receiving at its gate the control signal UP from phase comparator circuit; an n channel MOS transistor 3f connected between output node 3a and a node 3e and receiving at its gate the control signal/DOWN from phase comparator circuit 2; and a constant current circuit 3e connected between node 3e and a ground node 1b receiving the ground potential GND for sinking a prescribed constant current. When control signal UP is at the L level and the control signal/DOWN is at the L level, charge pump circuit 3 supplies charges to node 3, and when control signal UP is at the H level and the control signal/DOWN is at the H level, it sinks charges from node 3a. Loop filter 4 serves as a lowpass filter for removing a high frequency component of potential change at the output node 3a of charge pump circuit 3. Loop filter 4 includes a resistance element 4b connected between output node 3a and node 4a; a resistance element 4d connected between nodes 4a and 4c; and a capacitor 4e connected between node 4c and the ground node 1b. Resistance elements 4b and 4d and the capacitor 4e constitute an RC lowpass filter, and a potential VP corresponding to the potential on output node 3a of charge pump circuit 3 is output from node 4a.

Brief Summary Text (9):
Current adjusting potential output circuit 5 includes a p channel MOS transistor 5b connected between power supply node 1a and node 5a and having its gate connected to node 4a of loop filter 4; and an n channel MOS transistor 5c connected between node 5a and ground node 1b and having its gate connected to node 5a. The n channel MOS transistor 5c has its gate and drain connected to each other and operates in a saturation region, and therefore it sets the potential at gate 5a in accordance with a current applied from p channel MOS transistor 5b, in accordance with square-law characteristic of (Ids=.beta.(Vgs-Vth).sup.2).

Brief Summary Text (10):
Ring oscillator 6 includes an odd-number of inverters 6a connected in a ring shape, each having driving current (operational current) adjusted in accordance with output potentials VP and VN. These odd-number of inverters 6a have the same structure and denoted by the same reference character. Inverter 6a includes a current adjusting p channel MOS transistor 6ab connected between power supply node 1a and a node 6aa and receiving at its gate the output potential VP from loop filter 4; a p channel MOS transistor 6ae connected between node 6aa and an output node 6ac and having its gate connected to input node 6ad; an n channel MOS transistor 6ad connected between

output node 6ac and a node 6af and having its gate connected to input node 6ad; and a current adjusting n channel MOS transistor 6ah connected between node 6af and ground node 1b and receiving at its gate the output potential VN from current adjusting potential output circuit 5. The operation will be briefly described.

Brief Summary Text (15):
By the above described series of operations, the external clock extCLK and the internal clock intCLK have their phases and/or frequencies made equal by the PLL circuit. The state in which internal clock intCLK has the same frequency and phase as those of external clock extCLK will be referred to as a state in which internal clock intCLK is locked in to the external clock extCLK.

Brief Summary Text (16):
In the conventional PLL circuit shown in FIG. 1, the output potential VP of loop filter 4 is directly applied to p channel MOS transistor 5b of current adjusting potential generating circuit and to the gate of p channel MOS transistor 6ab of inverter 6a of ring oscillator 6. Therefore, only with a small fluctuation of output potential VP, the current flowing through p channel MOS transistors 5b and 5ab changes significantly in accordance with the square-law characteristic. Accordingly, current flowing through n channel MOS transistor 5c largely varies, and current flowing through MOS transistor 6ah (MOS transistor for adjusting current of inverter 6a), constituting a current mirror circuit together with the MOS transistor 5c, changes significantly. By the change in current, the delay time of inverter 6a much changes. As a result, only by a small fluctuation of output potential VP from loop filter 4, internal clock intCLK output from ring oscillator 6 changes significantly. Even after the internal clock intCLK is locked in to the external clock extCLK, frequency/phase of internal clock intCLK much fluctuates because of small potential fluctuation at output node 3a of charge pump circuit 3. Accordingly, there arises a problem that the frequency of internal clock intCLK much fluctuates around the external clock extCLK, namely, the jitter of internal clock intCLK becomes larger.

Brief Summary Text (17):
When supply of the external clock extCLK is interrupted, the PLL circuit changes the output potential VP of loop filter 4 so as to lock the internal clock intCLK in the interrupted external clock extCLK, and hence the output potential VP changes significantly. Accordingly, when the external clock extCLK is applied again, it takes long time to lock the internal clock intCLK again in the external clock extCLK.

Brief Summary Text (19):
Further, if the power supply potential VCC fluctuates much, the fluctuation in gate-source voltage (gate-to-source voltage) of p channel MOS transistors 5b and 6ab for current adjustment becomes larger, current flowing through MOS transistors 6ab and 6ah for current adjustment changes accordingly, and frequency of internal clock intCLK changes continuously. Therefore, it becomes difficult to lock the internal clock intCLK in the external clock extCLK, and hence it becomes difficult to generate the internal clock intCLK which has its phase synchronized with the external clock extCLK.

Brief Summary Text (25):
A still further object of the present invention is to provide a power supply potential supplying circuit capable of supplying an internal power supply potential of which fluctuation is suppressed.

Brief Summary Text (26):
According to a first aspect, the present invention includes a difference adjusting circuit for detecting difference in frequency and phase of the external clock signal as the first signal and the internal clock signal as the second signal and for outputting a signal for reducing the difference in accordance with the result of detection; a differential amplifying circuit for differentially amplifying the output signal from the difference adjusting circuit and a feedback potential; and an internal clock signal generating circuit of which operational current is adjusted in accordance with the output signal from the differential amplifying circuit. The feedback potential is generated at a connection portion between a current supplying element supplying current in accordance with the output signal from the differential

amplifying circuit and a resistance element connected between the current supplying element and a power supply (ground) node.

Brief Summary Text (27):
According to a second aspect of the present invention, the semiconductor device includes a difference adjusting circuit for detecting difference in at least one of phase and frequency between an internal clock signal and an external clock signal and for generating a control signal for reducing the detected difference, a current adjusting circuit for adjusting operational current of the internal clock signal generating circuit in accordance with the output signal from the difference adjusting circuit, and a holding circuit detecting a locking state of the external clock signal and the internal clock signal for holding the output signal from the difference adjusting circuit when the locking state is detected.

Brief Summary Text (29):
According to a fourth aspect of the present invention, the semiconductor device includes a comparing circuit for comparing a difference between a reference potential and an internal potential and for generating an analog signal indicative of the result of comparison; a digital converting circuit for converting an analog output signal from the comparing circuit to a digital signal; an analog charge pump circuit for adjusting gate potential of a current control transistor in accordance with the analog signal from the comparing circuit; a digital charge pump circuit for adjusting gate potential of the current control transistor in accordance with the output signal from the digital converting circuit; and a current drive transistor supplied with current from the current control transistor for supplying the current to an internal power supply node in accordance with the difference between an internal power supply potential and the reference potential.

Brief Summary Text (30):
According to a fifth aspect of the present invention, the semiconductor device includes a first current drive transistor connected between an external power supply node and an internal power supply node and receiving at its gate a reference potential; a second current drive transistor receiving at its gate the reference potential for supplying current from the external power supply node; a comparing circuit for comparing difference between the internal power supply potential and the reference potential and outputting an analog signal indicative of the difference; a digital converting circuit for converting an analog output signal from the comparing circuit to a digital signal; a third current drive transistor connected between the second current drive transistor and the internal power supply node; an analog charge pump circuit for adjusting gate potential of the third current drive transistor in accordance with the analog signal from the comparing circuit; and a digital charge pump circuit for adjusting gate potential of the third current drive transistor in accordance with an output signal from the digital converting circuit.

Brief Summary Text (34):
In the invention in accordance with the fourth aspect, the gate potential of the current control transistor is adjusted combining analog and digital manners, so that the supply current of the current control transistor can be adjusted in accordance with the fluctuation of the internal power supply potential, the overshoot and the undershoot of the internal power supply potential can be suppressed, and hence the internal power supply potential can be maintained stably at a constant potential level.

Brief Summary Text (35):
In the invention in accordance with the fifth aspect, a current is supplied constantly to the internal power supply node in accordance with the difference between the reference potential and the internal power supply potential, and the gate potential of still another third current drive transistor is controlled in analog manner or digital manner in accordance with the potential at the internal power supply node. Therefore, the amount of current supplied to the internal power supply node can be adjusted in accordance with the change in the internal power supply potential, and hence the internal power supply potential can be maintained stably at a prescribed potential level.

Drawing Description Text (3):

FIG. 1 shows an example of a structure of a conventional PLL circuit.

Drawing Description Text (7):
FIG. 5 shows a structure of an internal power supply potential generating circuit shown in FIG. 2.

Drawing Description Text (8):
FIGS. 6 and 7 are timing charts representing the operation of the internal power supply potential generating circuit shown in FIG. 5.

Drawing Description Text (30):
FIG. 27 shows a still further structure of the internal power supply potential generating circuit.

Drawing Description Text (31):
FIG. 28 shows a still further structure of the internal power supply potential generating circuit.

Drawing Description Text (32):
FIG. 29 shows a still further structure of the internal power supply potential generating circuit.

Drawing Description Text (34):
FIG. 31 shows a still further structure of the internal power supply potential generating circuit.

Drawing Description Text (35):
FIG. 32 shows a still further structure of the internal power supply potential generating circuit.

Detailed Description Text (4):
SRAM 300 operates in synchronization with the external clock signal extCLK, receives the control signal CTRL and the address signal Ai applied from microprocessor 200, and performs memory cell selecting operation and data input/output operation. SRAM 300 includes an internal power supply potential generating circuit 310a (see FIG. 4) for generating and outputting to an internal power supply node 300c an internal power supply potential intVCC (for example, 3 V) from the external power supply potential extVCC (for example, 5 V) applied to external power supply node 300a and the ground potential GND (0 V) which is another external power supply potential applied to a ground node 300b; an internal power supply potential generating circuit 310b for clocks for generating and outputting to an internal power supply node 300d for clocks an internal power supply potential intVCC based on the external power supply potential extVCC and the ground potential GND; and an internal clock signal synchronizing circuit 320 (see FIG. 6) which operates using the internal power supply potential intVCC on the internal power supply node 300d for clocks as one operational power supply potential and outputs internal clock signal intCLK, .phi.1 and .phi.2 synchronized with the external clock signal extCLK. The internal power supply potential generating circuit 310b has similar structure as internal power supply potential generating circuit 310a, and it down-converts the external power supply potential extVCC to generate the internal power supply potential intVCC. In the present embodiment, the internal clock signal synchronizing circuit 320 is provided by a PLL circuit, as will be described in detail later.

Detailed Description Text (7):
SRAM 300 further includes a memory cell array 350 in which SRAM cells are arranged in a matrix of rows and columns, and which includes memory cells 331 each of which stores 1 bit of data. A word line 352 is arranged corresponding each row of the memory cells, and the memory cells arranged in the corresponding row are connected to each word line 352. A bit line pair 353 is arranged corresponding to each column of the memory cells, and the memory cells of the corresponding column are connected to each bit line pair 353. The bit line pair 353 has bit lines 353a and 353b for transmitting mutually complementary data signals. To the bit line pair 353, a bit line equalizing circuit 354 for equalizing the potentials BL and/BL of bit lines 353a and 353b at the level of the internal power supply potential intVCC in synchronization with the internal clock signal .phi.1 is provided. The bit line

equalizing circuit 354 is activated and supplies the internal power supply potential intVCC to the bit lines 353a and 353b, when the memory cell array 350 is not selected, that is, when the internal clock signal .phi.1 is at the L level, the word line 352 and the bit line pair 353 are not selected.

Detailed Description Text (8):
Memory cell 351 includes a load element 351c of a high resistance connected between internal power supply node 300c and storage node 351a; a load element 351d of a high resistance connected between internal power supply node 300c and storage node 351b; an n channel MOS drive transistor 351e connected between storage node 351a and ground node 300b and having its gate connected to storage node 351b; an n channel MOS drive transistor 351h connected between storage node 351b and ground node 300d and having its gate connected to storage node 351a; an n channel MOS access transistor 351g connected between bit line 353a and storage node 351a and having its gate connected to word line 352; and an n channel MOS access transistor 351f connected between bit line 353b and storage node 351b and having its gate connected to word line 352. Each of the load elements 351c and 301d is formed by a high resistance polycrystalline silicon or by a p channel MOS transistor (for example, a thin film transistor) having its gate connected to the corresponding storage node 351a or 351b.

Detailed Description Text (9):
Bit line equalizing circuit 354 includes a p channel precharge transistor 354a connected between internal power supply node 300c and bit line 353a and receiving at its gate the internal clock signal .phi.1; a p channel precharge transistor 354b connected between internal power supply node 300c and bit line 353b and receiving at its gate the internal clock signal .phi.1; and a p channel equalize transistor 354c connected between bit line 353a and bit line 353b and receiving at its gate the internal clock signal .phi.1. These transistors 354a, 354b and 354c are rendered conductive when the internal clock signal .phi.1 attains to the L level.

Detailed Description Text (25):
Bit line equalizing circuit 354 is rendered active in synchronization with the fall of internal clock signal .phi.1, and it equalizes and precharges the bit line pair 353 to the level of the internal power supply potential intVCC.

Detailed Description Text (27):
FIG. 4 shows a structure of a portion related to 1 bit of address signal of address buffer 330 shown in FIG. 2. Referring to FIG. 4, address buffer 330 includes an inverter 330a for inverting an external address signal Ai when activated; a p channel MOS transistor 330b responsive to activation of internal clock signal .phi.1 (L level) for supplying current from external power supply node 300a to one operational power supply node of inverter 330a; an n channel MOS transistor 330c responsive to activation of an inverted signal/.phi.1 of internal clock signal .phi.1 for forming a current path between another power supply node of inverter 330a and ground node 300b;an inverter 330d receiving an output signal from inverter 330a; and a clock inverter 330e activated when internal clock signal .phi.1 is at the high level, for inverting and buffering the output signal from inverter 330d for transmission to the input portion of inverter 330d.

Detailed Description Text (30):
MOS transistor 330b is connected to external power supply node 300a, and in order to render MOS transistor 330b non-conductive, the H level of internal clock signal .phi.1 must be increased to the level of the external power supply potential extVCC. This can be readily implementing by using a simple level converting circuit. Level conversion is not necessary for the inverted signal/.phi.1.

Detailed Description Text (32):
FIG. 5 is a circuit diagram showing the structure of the internal power supply potential generating circuit 310a shown in FIG. 2. Referring to FIG. 5, internal power supply potential generating circuit 310a includes a constant voltage circuit 311 receiving a current from current supply node 312 for outputting an internal power supply potential intVCC at a level of a constant reference potential Vref on internal power supply node 300c, and a current supplying circuit 316 adjusting the amount of current supplied to current supply node 312 in accordance with the

difference between internal power supply potential intVCC and the reference potential Vref. Here, the potential is measured with reference to the ground potential.

Detailed Description Text (33):
Constant voltage circuit 311 includes a reference potential generating circuit 313 receiving external power supply potential extVCC and the ground potential GND for outputting a constant reference potential Vref (for example, 3 V when extVCC=5 V) which is not influenced by the fluctuation in the external power supply potential extVCC; a differential amplifying circuit 314 comparing the reference potential Vref from reference potential generating circuit 313 and internal power supply potential intVCC for outputting a driver control signal DRV corresponding to the difference therebetween; and a driver transistor 315 constituted by a p channel MOS transistor connected between current supply node 312 and internal power supply node 300c and having its gate connected to receive the driver control signal DRV from differential amplifying circuit 314. When the internal power supply potential intVCC is lower than the reference potential Vref, differential amplifying circuit 314 lowers the potential level of driver control signal DRV. If the internal power supply potential intVCC is higher than the reference potential Vref, the differential amplifying circuit 314 increases the potential level of driver control signal DRV. The driver control signal DRV changes in an analog manner.

Detailed Description Text (34):
Reference potential generating circuit 313 includes a constant current circuit 313b connected between external power supply node 300a and reference potential node 313a for supplying a constant current regardless of the fluctuation of the external power supply potential extVCC, and a resistance element 313c connected between reference potential node 313a and ground node 300b.A reference potential Vref is output on reference potential node 313a.

Detailed Description Text (35):
Constant current circuit 313b includes a p channel MOS transistor 313bc connected between external power supply node 300a and node 313ba and having its gate connected to node 313bb; and n channel MOS transistor 313be connected between node 313ba and ground node b and having its gate connected to node 313bd; a resistance element 313bf connected between external power supply node 300a and node 313bb; a p channel MOS transistor 313bg connected between nodes 313b and 313bd and having its gate connected to node 313ba; an n channel MOS transistor 313bh connected between node 313bd and ground node 300b and having its gate connected to node 313bd; and a p channel MOS transistor 313bi connected between external power supply node 300a and reference potential node 313a and having its gate connected to node 313bb.

Detailed Description Text (36):
In constant current circuit 313b, resistance element 313bf has relatively large resistance value, and supplies small current to MOS transistors 313bg and 313bh. MOS transistors 313bh and 313be constitute a current mirror circuit, and mirror current of the current flowing through MOS transistor 313bh flows through MOS transistor 313be. The current flowing through MOS transistor 313be is supplied from MOS transistor 313bc. Current drivability of MOS transistor 313bc is made large, and source-gate voltage of MOS transistor 313bc, that is, potential difference between internal power supply node 300a and node 313bb is set to the absolute value .vertline.vthp.vertline. of the threshold MOS transistor 313bc. Therefore, the current I flowing through resistance element 313bf is given by .vertline.Vthp.vertline./R (313ef), where R (313ef) represents resistance value of resistance element 313ef. The current I has a constant current value which is not dependent on the external power supply potential extVCC. When the current I increases, the current flowing through MOS transistors 313bg and 313bh increases, the current flowing through MOS transistor 313be increases, the potential at node 313ba increases (as the drain current of MOS transistor 313be is determined by the potential at node 313ba), the current flowing through MOS transistor 313g is lowered accordingly, the potential at node 313bb is increased, and the current flowing through MOS transistor 313bc is lowered. When the current flowing through resistance element 313bf lowers, the potential at node 313ba lowers, the conductance of MOS transistor 313bg is increased, larger amount of current is drawn out from node 313bb, the potential at node 313bb is decreased accordingly, and the current is

increased through MOS transistor 313b. By the feedback control of MOS transistors 313bg, 313bh and 313be, the current flowing through MOS transistor 313bc and resistance element 313bf is made constant. The node 313bd is connected to the gate of MOS transistors 313bi. Therefore, a constant current flows through MOS transistor 313bi, as in MOS transistor 313bc. Reference potential Vref is determined by the current supplied from MOS transistor 313bi and the resistance value of resistance element 313c. Since the current flowing through MOS transistor 313bi has a constant value not dependent on the external power supply potential extVCC, the reference potential Vref also has a constant potential not dependent on the external power supply potential extVCC.

Detailed Description Text (37):
Differential amplifying circuit 314 includes a p channel MOS transistor 314c connected between external power supply node 300a and an output node 314a outputting a driver control signal DRV and having its gate connected to node 314b; an n channel MOS transistor 314e connected between nodes 314a and 314d and having its gate connected to receive reference potential Vref; a p channel MOS transistor 314f connected between external power supply node 300a and node 314b and having its gate connected to node 314b; an n channel MOS transistor 314g connected between nodes 314b and 314d and having its gate connected to receive internal power supply potential intVCC; and an n channel MOS transistor 314h connected between node 314d and ground node 300b and having its gate connected to external power supply node 300a. MOS transistors 314c and 314f constitute a current mirror circuit, MOS transistors 314e and 314g constitute a differential stage for comparing potentials applied to their gates, and MOS transistor 314h serves as a constant current source for supplying a relatively large constant current in accordance with the external power supply potential extVCC applied to the gate. The differential amplifying circuit 314 has a structure of a current mirror type differential amplifying circuit, of which positive input (+) is the gate of the MOS transistor 314g and its negative input (-) is the gate of the MOS transistor 314e. The signal DRV changes in a digital manner.

Detailed Description Text (38):
Current supplying circuit 316 adjusts the current supplied to current supply node 312 in accordance with the difference between internal power supply potential intVCC and reference potential Vref so that undershoot and overshoot of internal power supply potential intVCC with respect to the reference potential Vref is minimized. The current supplying circuit 316 includes a p channel current control transistor 316a connected between external power supply node 300a and current supply node 312; and a current control circuit 316b receiving the reference potential Vref from reference potential generating circuit 313 and the internal power supply potential intVCC on internal power supply node 300c for adjusting the gate potential Vg of p channel current control transistor 316a. The current control circuit 316b lowers the gate potential Vg of current control transistor 316a when the undershoot of the internal power supply potential intVCC with respect to the reference potential Vref becomes larger, and if the overshoot becomes larger, it increases the gate potential Vg of current control transistor 316a.

Detailed Description Text (39):
Current control circuit 316b includes a comparing circuit 316bc for comparing internal power supply potential intVCC with the reference potential Vref; a charge pump circuit 316bg for adjusting gate potential Vg of current control transistor 316a in accordance with an output potential Va from comparing circuit 316bc; and a loop filter 316bi connected between the gate of current control transistor 316a and ground node 300b.Comparing circuit 316bc includes differential amplifying circuit 316ba and 316bb having the same structure as differential amplifying circuit 314 included in constant voltage circuit 311. Each of the differential amplifying circuit 316ba and 316bb outputs a signal Va which attains to the L level when the internal power supply potential intVCC is higher than the reference potential Vref and attains to the H level if the internal power supply potential intVCC is lower than the reference voltage Vref.

Detailed Description Text (40):
Charge pump circuit 316bg includes a p channel MOS transistor 316be connected between external power supply node 300 and a node 316bd connected to the gate of

current control transistor 316a and having its gate connected to the output of differential amplifying circuit 316b, and an n channel MOS transistor 316bf connected between node 316bd and ground node 300b and having its gate connected to receive output potential Va of differential amplifying circuit 316bd.

Detailed Description Text (41):
Loop filter 316bi includes a capacitor 316bh connected between node 316bd and ground node 300b,and suppresses an abrupt change in gate potential Vg. The operation of internal power supply potential generating circuit 310a shown in FIG. 5 will be briefly described.

Detailed Description Text (42):
When the internal power supply potential extVCC is within the range of about 5 V to about 2 V, reference potential generating circuit 313 operates stably, a constant current is supplied from current control circuit 316b, and the reference potential Vref output from reference potential generating circuit 313 is kept at a constant potential level accordingly, regardless of the fluctuation of external power supply potential extVCC. Differential amplifying circuit 314 receives the reference potential Vref and internal power supply potential intVCC, and compares this. When internal circuitry such as decoders 340a and 340b connected to internal power supply node 300c and memory cell 351 operate and consume current and the internal power supply potential intVCC becomes lower than the reference potential Vref (that is, when there is an undershoot), the driver control signal DRV output from output node 314a lowers and increases the conductance of drive transistor 315. Drive transistor 315 supplies a large amount of current to internal power supply node 300c in accordance with the increased conductance, thereby increasing internal power supply potential intVCC. When internal power supply potential intVCC becomes higher than the reference potential Vref by the current supply (when there is an overshoot) differential amplifying circuit 314 raises the driver control signal DRV and reduces conductance of driver transistor 315, so that the amount of current supply to internal power supply node 300c is reduced. When the internal circuit is in operation at this time, the internal power supply potential intVCC is consumed by the operating internal circuitry, and hence it becomes lower. When the current supply to current supplying node 312 is small, the internal power supply potential intVCC which has become lower than the reference potential Vref does not increase at high speed, and hence the undershoot becomes larger. Meanwhile, if the current supplied to current supply node 312 is increased, the internal power supply potential intVCC increases at high speed, and hence the overshoot becomes larger. Generation of the undershoot and the overshoot will be described with reference to FIGS. 6 and 7.

Detailed Description Text (43):
FIG. 6 is a timing chart showing the operation of the current supplying circuit 316 when there is a large undershoot of internal power supply potential intVCC. If the undershoot of internal power supply potential intVCC becomes larger from time t1 to t2 as shown in (a) of FIG. 6, the output potential Va from differential amplifying circuits 316ba and 316bb included in comparing circuit 316bc is kept at the H level for a long period of time as shown at (b) of FIG. 6, and the time period in which p channel MOS transistor 316bb included in charge pump circuit 316bg is rendered non-conductive and n channel MOS transistor 316bf is rendered conductive becomes longer. Therefore, as shown in (c) of FIG. 6, the potential Vg on current control transistor 316a is discharged by the conduction of MOS transistor 316bf of charge pump circuit 316bg and lowers significantly. As a result, conductance of current control transistor 316a is increased, the current Is supplied from external power supply node 300a to power supply node 312 becomes larger as shown in (d) of FIG. 6, and hence the internal power supply potential intVCC is increased at high speed. From time t2 to t3, the internal power supply potential intVCC increases to be higher than the reference potential Vref because of this large amount of current. Accordingly, by the function of differential amplifying circuit 316bc, gate potential Vg is kept increased in this period and the amount of current supplied is reduced. At this time, since the difference between internal power supply potential VCC and the reference potential Vref is small, the amount of change of current Is supplied to current supply node 312 through current control transistor 316a is small, and hence the undershoot of internal power supply potential intVCC in the period from time t3 to t4 is made smaller. After the time point t2 where large

undershoot of internal power supply potential intVCC is suppressed, the period in which L level and H level of output potential Va from each of differential amplifying circuit 316ba and 316bb is made approximately the same. Therefore, by the function of the loop filter 316bi, the gate potential Vg of current control transistor 316a and supply current Is do not change much as shown in (c) and (d) of FIG. 6, but these are maintained at approximately constant values. During this period, the internal power supply potential intVCC vibrates with a small amplitude. However, the vibration is smoothed because of a parasitic resistance or stabilizing capacitance incidental to the internal power supply node 300c, and an internal power supply potential intVCC at the level of the reference potential Vref is output.

Detailed Description Text (44):
The operation when the overshoot of internal power supply potential intVCC becomes larger will be described with reference to the timing chart of FIG. 7.

Detailed Description Text (45):
When the overshoot of the internal power supply potential intVCC becomes large at time t1 to t2 in FIG. 7 at (a), the output potential Va of differential amplifying circuits 316ba and 316bb of comparing circuit 316bc is kept at the L level for a long period of time as shown at (b) of FIG. 7, and accordingly, the period in which p channel MOS transistor 316be is rendered conductive and n channel MOS transistor 316bf is rendered non-conductive in charge pump circuit 316bg becomes longer. By the p channel MOS transistor 316be which is set to the conductive state, the gate potential Vg of current control transistor 316a increases significantly as shown in (c) of FIG. 7. Consequently, the current Is supplied through current control transistor 316a to current supply node 312 becomes smaller as shown in FIG. 7 at (d), and increase in potential of internal power supply potential intVCC is suppressed. By the reduced supply current, the internal power supply potential intVCC lowers, and if it becomes the reference potential Vref at time t2, the gate potential Vg is again lowered by charge pump circuit 316bg, so that the supply current Is is increased a little to suppress the undershoot. Consequently, overshoot in a period from t3 to t4 can be made sufficiently small. In the stable state after the time point t2, the period in which the output potential Va from differential amplifying circuit 316ba and 316bb is kept at the L level and H level are made shorter to be approximately equal to each other as shown in FIG. 7 at (d), and therefore supply potential Is and the gate potential Vg of current control transistor 316a hardly change as shown in (c) and (d) of FIG. 7. Consequently, in the similar manner as at the time of generation of large undershoot, the internal power supply potential intVCC is maintained at the level of the reference potential Vref.

Detailed Description Text (46):
As described above, by adjusting the amount of current supplied to current supply node 312 in accordance with the difference between internal power supply potential VCC and reference potential Vref, even when the drive transistors 315 performs on/off operation in digital manner by using the control signal DRV output from differential amplifying circuit 314, the undershoot/overshoot can be suppressed quickly and hence the internal power supply potential intVCC can be returned to the prescribed reference potential Vref level.

Detailed Description Text (49):
When comparison signal/UP is at the L level and comparison signal DOWN is at the L level, charge pump circuit 322 supplies charges to charging/discharging node 322a, and when comparison signal/UP is at the H level and comparison signal DOWN is at the H level, it sinks charges from charge/discharge node 322a. Charge pump circuit 322 includes a constant current circuit 322c connected between internal power supply node 300c and node 322b; a p channel MOS transistor 322d connected between node 322b and charging/discharging node 322a and having its gate connected to receive the comparison signal/UP from phase comparator circuit 321; an n channel MOS transistor 322f connected between charging/discharging node 322a and node 322e and having its gate connected to receive the comparison signal DOWN from phase comparator circuit 321; and a constant current circuit 322g connected between node 322e and ground node 300b.Constant current circuit 322c and 322g have the same structure as the constant current circuit 313b of reference potential generating circuit 313 included in internal power supply potential generating circuit 310a shown in FIG. 5. However,

since constant current circuit 322g sinks current, the conductivity type of the transistors and the polarities of potentials applied to power supply nodes are all opposite to those of the constant current circuit 313b shown in FIG. 5. By the constant current circuit 322c and 322g, a constant current is supplied, regardless of the fluctuations in internal power supply potential intVCC and the ground potential GND.

Detailed Description Text (51):
Operational amplifier 323d includes a first node 323da connected through loop filter 323c to charging/discharging node 322a, a second input node 323db receiving the feedback potential Vf, and an amplifying output node 323bc for outputting p channel power supply control signal V.sub.p.

Detailed Description Text (53):
Operational amplifier 323d has similar structure as the differential amplifying circuit 314 included in the internal power supply potential generating circuit 310a shown in FIG. 5. However, the output signal from operational amplifier 323 changes in an analog manner.

Detailed Description Text (54):
The p channel current control circuit 323e includes a p channel MOS transistor 323eb connected between internal power supply node 300d for clocks and node 323ea and having its gate connected to the amplifying output node 323dc of operational amplifier 323d, a resistance element 323eb connected between node 323ea and ground node 300b, and a capacitor 323ee connected parallel to resistance element 323eb between node 323ea and ground node 300b. Node 323ea is connected to the second input node 323db of operational amplifier 323d and outputs the feedback potential Vf. Resistance element 323dd and capacitor 323ee has a function of stably generating the potential Vf of node 323ea.

Detailed Description Text (55):
The n channel current control circuit 323f includes a p channel MOS transistor 323fb connected between internal power supply node 300d for clocks and the node 323fa at which the n channel current control signal Vn is output and having its gate connected to the amplifying output node 323dc of operational amplifier 323d, and an n channel MOS transistor 323fc connected between node 323fa and ground node 300b and having its gate connected to node 323fa.

Detailed Description Text (57):
Inverter 324a includes a p channel current control transistor 324ab connected between internal power supply node 300d for clocks and node 324aa and having its gate connected to amplifying output node 323d of operational amplifier 323d; a p channel MOS transistor 324ae connected between node 324aa and output node 324ac and having its gate connected to internal node 324ad; an n channel MOS transistor 324ag connected between output node 324ac and node 324af and having its gate connected to input node 324ab; and an n channel current control transistor 324ah connected between node 324af and ground node 300b and having its gate connected to receive the n channel current control signal Vn. Three stages of inverters 324a are connected in a ring. The internal clock signal .phi.2 is output from the first stage of inverter 324a, the internal clock signal .phi.1 is output from the second stage of inverter 324a and the internal clock signal intCLK is output from the last stage (third stage) of inverter 324a. The operation of the external clock signal synchronizing circuit 320 shown in FIG. 8 will be described.

Detailed Description Text (59):
Meanwhile, when the potential level of p channel current control signal V.sub.p increases, the amount of current flowing through p channel MOS transistor 323fb in n channel current control circuit 323f becomes smaller, and accordingly, the potential level of n channel current control signal Vn output from node 323fa becomes lower. Finally, the n channel current control signal Vn settles at a potential level at which the current flowing through n channel MOS transistor 323fc becomes equal to the current flowing through p channel MOS transistor 323fb (the operation is the same as in the conventional PLL circuit shown in FIG. 1).

Detailed Description Text (63):

FIG. 9 schematically shows a structure of phase comparing circuit 321 shown in FIG. 8. In FIG. 9, structure of that portion which performs only phase adjustment at a rise of the external clock signal and the internal clock signal, of the phase comparing circuit 321 is shown. A circuit having similar structure as that shown in FIG. 9 is provided which operates in response to the fall of the external clock signal extCLK and the internal clock signal intCLK. Referring to FIG. 9, phase comparing circuit 321 includes a D flipflop 321a having a D input coupled to internal power supply node 300c, a clock input CP receiving external clock signal extCLK, complementary output nodes Q and/Q, and a reset input/R; a D flipflop 312b having a D input coupled to internal power supply node 300c, a clock input CP receiving internal clock signal intCLK, complementary output nodes Q and/Q and a reset input/R; an NAND gate 321c receiving a signal from output Q from D flipflop 321a and an output signal from output Q of D flipflop 312b; an inverter 321d inverting an output signal from output/Q of D flipflop 321a; an inverter 321e inverting a signal from output/Q of D flipflop 321b; an NOR gate 321f receiving a signal from output/Q of D flipflop 321a and an output signal from inverter 312e; an inverter 321g inverting an output signal from NOR gate 321f; and an NOR gate 321h receiving an output signal from output/Q of D flipflop 321d and an output signal from inverter 321a. The control signal/UP is output from inverter 321g, and control signal DOWN is output from NOR gate 321h. The output signal from NAND gate 321c is applied to reset input/R of D flipflop 321a and 321b. The operation will be briefly described.

Detailed Description Text (80):
Further, since internal clock signal intCLK is generated by internal clock signal synchronizing circuit 320 using internal power supply potential intVCC which is more stable than external power supply potential extVCC as operational power supply potential, fluctuation of internal clock signal intCLK can be suppressed, internal clock signal intCLK can be readily locked in external clock signal extCLK, and jitter of the internal clock signal intCLK after locked in can be made smaller.

Detailed Description Text (81):
Since internal power supply potential generating circuit 310b for clocks supplying internal power supply potential intVCC for generating the internal clock is provided separately from the internal power supply potential generating circuit 310a supplying internal power supply potential intVCC to other internal circuits, the internal power supply potential intVCC for generating internal clock signal is made stable and not influenced by the operation of other internal circuits. Therefore it becomes easier to lock internal clock signal intCLK in external clock signal extCLK, and the jitter of the internal clock signal intCLK after locked in is made smaller.

Detailed Description Text (82):
Further, in the internal power supply potential generating circuits 310a and 310b,current supplying circuit 316 supplying current to current supply node 312 is provided to make smaller the undershoot and overshoot of internal power supply potential intVCC with respect to the reference potential Vref, and hence stable internal power supply potential intVCC can be obtained.

Detailed Description Text (88):
The p channel current control circuit 323e for generating feedback potential Vf in accordance with the output potential of operational amplifier 323d includes a p channel MOS transistor 323eb connected between internal power supply node 300d and node 323ea and receiving at its gate an output potential from operational amplifier 323d; a transfer gate 323eh connected between nodes 323ea and 323ec and selectively set to the conductive state in response to hold signals HD and/HD; and an n channel MOS transistor 323ei connected between node 323ec and ground node 300b and receiving at its gate a switching potential Vr from resistance value switching circuit 323h. Transfer gate 323eh includes a p channel MOS transistor 323ef connected between nodes 323ea and 323ec and receiving at its gate the hold signal HD, and an n channel MOS transistor 323eg connected parallel to p channel MOS transistor 323ef between nodes 323ea and 323ef and receiving at its gate the hold signal/HD.

Detailed Description Text (89):
The structure of resistance value switching circuit 323h will be described later. These circuits increases the switching potential Vr when the external power supply

potential extVCC and ground potential GND are applied, and thereafter lowers and maintains the switching potential Vr at a prescribed low potential. Node 323ea is connected to a second input node 323db of operational amplifier 323d.

Detailed Description Text (94):
FIG. 13A shows a specific structure of the resistance value switching circuit 323h shown in FIG. 11. Referring to FIG. 13A, resistance value switching circuit 323h outputs a resistance value switching potential Vr to output node 323ha.The output node 323ha is connected to external terminal 323hb. As shown in FIG. 13B, at time to, external power supply ext and ground potential GND are turned on and external power supply potential extVCC (for example, 5 V) is applied, the switching potential Vr applied to external terminal 323hb is also set to the same potential level as the external power supply potential. When a prescribed time period passes from power on and the internal circuitry is stabilized, the resistance value switching potential Vr applied to external terminal 323hb is set to a potential (for example, 1 V) lower than the external power supply potential extVCC. Therefore, referring to FIG. 11, since the resistance value switching potential Vr is applied to the gate of n channel MOS transistor 323ei, the resistance value of MOS transistor 323ei is minimized when the power is turned on, and when the stable state is achieved, the resistance value is increased.

Detailed Description Text (95):
FIG. 14A shows another specific structure of resistance value switching circuit 323h shown in FIG. 11, and FIG. 14B shows the operational waveform thereof. Referring to FIG. 14A, resistance value switching circuit 323h includes a resistance element 323hd connected between external power supply node 300a and node 323hc, a resistance element 323he connected between node 323hc and output node 323ha, a resistance element 323hf connected between output node 323ha and ground node 300b,an n channel MOS transistor 323hh connected parallel to resistance element 323hd between external power supply node 300b and node 323hc and having its gate connected to external terminal 323hg, and an n channel MOS transistor 323hj connected between node 323hc and output node 323ha parallel to resistance element 323he and having its gate connected to external terminal 323hi.

Detailed Description Text (96):
As in FIG. 14B, when power is turned on at time t0, external power supply potential extVCC is applied to external terminals 323hg and 323hi at this time. In response, MOS transistors 323hh and 323hj are both rendered conductive. The resistance value of resistance element 323hf is made sufficient larger than the on resistance of MOS transistor 323hh and 323hj. Therefore, switching potential Vr from output node 323ha is set to the level of the external power supply potential extvcc, as the resistance elements 323hd and 323he are short-circuited by the MOS transistors 323hh and 323hj. After the lapse of a prescribed time period, external power supply potential extVCC is applied to one of the external terminals 323hg and 323hi at time t1, and the ground potential GND is applied to the other. In FIG. 14B, the ground potential GND is shown to be applied to external terminal 323hg. In this state, one of the MOS transistors 323hh and 323hj is rendered non-conductive. Therefore, when resistance elements 323hd, 323he and 323hf all have the same resistance values, the resistance value between external power supply node 300a and output node 300ha is made equal to the resistance value between output node 323ha and ground node 300b,and switching potential Vr is set to the potential level of approximately extVCC/2.

Detailed Description Text (97):
After the lapse of another time period at time t2, the ground potential GND is supplied to external terminals 323hg and 323hi, and MOS transistors 323hh and 323hj are rendered non-conductive. In this state, resistance elements 323hd, 323he and 323f are connected in series between external power supply node 300a and ground 300b, and since these resistance elements have the same resistance value, switching potential Vr is set to the potential level of extVCC/3.

Detailed Description Text (98):
FIG. 15A shows still another specific circuit structure of resistance value switching circuit 323h shown in FIG. 11 and FIG. 15B shows the operational waveform thereof. Referring to FIG. 15A, resistance value switching circuit 323h includes a resistance control circuit 323hk for adjusting potential level of switching

potential Vr in accordance with logical coincidence/incoincidence of comparing signals/UP and DOWN from phase comparing circuit 321, and a start up circuit 323hm for setting the resistance switching potential Vr to the external power supply potential extVCC for a prescribed time period at the time of power on. When the internal clock signal intCLK is not locked in external clock signal extCLK and therefore the time in which comparing signals/UP and DOWN are kept at the active state of L level and H level respectively is made long, the resistance control circuit 323hk sets the resistance value switching potential Vr output from output node 323ha approximately to the external power supply potential extVCC, and as the internal clock signal intCLK comes to be locked in external clock signal extCLK and the time period in which comparing signals/UP and DOWN are active becomes shorter, the circuit lowers the resistance value switching potential Vr and finally, it sets the resistance value switching potential to about 1 V. The resistance control circuit 323hk includes an EXOR circuit 323hn receiving comparing signals/UP and DOWN for determining coincidence/incoincidence therebetween, a constant current circuit 323hq connected between external power supply node 300a and node 323hp, a p channel MOS transistor 323hr connected between node 323hv and output node 323ha and receiving at its gate the output signal from NOR circuit 323hn, a resistance element 323ht connected between output node 323ha and node 323hs, and a p channel MOS transistor 323hu connected between node 323hs and ground node 300b and having its gate connected to ground node 300b.The resistance value of resistance element 323ht is made sufficiently larger than the on resistance of p channel MOS transistor 323hu. Therefore, MOS transistor 323hu operates in a diode mode, and the potential at node 323hs is maintained at the level of the absolute value of the threshold voltage Vth.

Detailed Description Text (99):
Start up circuit 323hm includes a power on reset signal generating circuit 323hv for outputting a power on reset signal/POR which is kept at the L level for a prescribed time period at a rise (power on) of the external power supply potential extVCC and thereafter set to the H level, and a p channel start up transistor 323hw connected between external power supply node 300a and output node 323ha and having its gate connected to receive the power on reset signal/POR.

Detailed Description Text (100):
When power is turned on and the potential level of external power supply potential extVCC rises at time t1, power on reset signal/POR is set to and kept at the L level for a prescribed time period, that is, up to the time point t2. During this period, p channel start up transistor 323hw is kept conductive, electrically short-circuits the external power supply node 300a and output node 323ha, and sets the switching potential Vr at the potential level of external power supply potential extVCC. When power on reset signal/POR rises to the H level at time t2, transistor 323hw is rendered non-conductive.

Detailed Description Text (101):
Constant current circuit 323hq has similar structure as constant current circuit 323c included in charge pump circuit 322, and at this time point, it is set to an operative state and supplies a constant current. At time t2, if there is large difference in phase/frequency between internal clock signal intCLK and external clock signal extCLK, the period in which comparing signal/UP and DOWN are kept active becomes longer. In that case, the period in which the output signal from EXOR circuit 323hn is at the L level becomes longer, and accordingly, the period in which p channel MOS transistor 323hr is conductive becomes longer. Therefore, in this period, the switching potential Vr output from output node 323ha is maintained at the potential level of external power supply potential extVCC.

Detailed Description Text (103):
As described above, when the external power supply potential extVCC and the ground potential GND are turned on, the switching potential Vr is set to the potential level of approximately the external power supply potential extVCC by the start up circuit 323hm. Thereafter, as the time passes, the potential level of switching potential Vr lowers by the function of resistance control circuit 323hk. Therefore, when the resistance value switching circuit 323h shown in FIG. 15A is used, the resistance value of n channel MOS transistor 323ei included in the power control circuit is the smallest at the time of power on, and the resistance value is

increased at the time of lock in.

Detailed Description Text (104):
As described above, since the resistance value of resistance transistor 323ei shown in FIG. 11 is minimized at the time of power supply and it is gradually increased thereafter, when there is a large difference in phase and frequency between internal clock signal intCLK and external clock signal extCLK at the time of power on, the current control signals V.sub.p and Vn fluctuate significantly with respect to the fluctuation in input potential Vin input to the first input node 323da of operational amplifier 323d shown in FIG. 11, and accordingly, driving current of the ring oscillator changes significantly. Therefore, internal clock signal intCLK is quickly pulled near to the external clock signal extCLK. Meanwhile, when the internal clock signal intCLK is about to be locked in clock signal extCLK, the resistance value of resistance transistor 323ei has been increased, the change in driving current of the ring oscillator relative to the change in control signals V.sub.p and Vn is made smaller, and internal clock signal intCLK changes relatively slowly. Therefore, it becomes easier to lock the internal clock signal intCLK in the external clock signal extCLK, and the jitter of the internal clock signal intCLK after lock in can be made smaller.

Detailed Description Text (105):
Further, when supply of the external clock signal extCLK to external clock signal input node 321a is stopped, hold signal HD is set to the H level and hold signal/HD is set to the L level. In response, the transfer gate 323j provided at the loop filter input portion is rendered non-conductive, and the output potential Vin of loop filter 323c is maintained for a prescribed time period. Similarly, in power supply control circuit 323e, transfer gate 323eh is rendered non-conductive, and the feedback potential Vf is kept at a constant potential level for a prescribed time period by the capacitor 323ee. Since input potential Vin and feedback potential Vf are held for a prescribed time period, the potential levels of current control signals Vp and Vn are held accordingly, and hence internal clock signal intCLK maintains the state it assume when the supply of the external clock signal extCLK is stopped, for this time period. Therefore, even when supply of the external clock signal extCLK is temporarily interrupted, the internal clock signal intCLK is output stably. When supply of the external clock signal extCLK is resumed, hold signals HD and/HD are set to the L level and H level, respectively, and transfer gates 323g and 323eh are rendered conductive. Consequently, the phase and frequency of the internal clock signal intCLK are adjusted in accordance with the phase/frequency of the external clock signal extCLK. In this case, the external clock signal extCLK is simply interrupted or disconnected temporarily and hence the phase and frequency of the newly applied external clock signal extCLK are not much different from those before interruption. Therefore, internal clock signal intCLK can be readily locked in the external clock signal extCLK.

Detailed Description Text (108):
Referring to FIG. 16, potential holding circuit 323i includes a potential storing circuit 323ia responsive to the hold signal HD for storing an input potential Vin on node 323da; a p channel MOS transistor 323ic connected between internal power supply node 300c and node 323ib; an operational amplifier 323id having an input receiving an analog signal AN from potential storing circuit 323ia and a potential at node 323ib and an output connected to the gate of p channel MOS transistor 323ic; a transfer gate 323ie1 connected between nodes 323ib and 323da and selectively set to the conductive state in response to hold signals HD and/HD; and a transfer gate 323if connected between nodes 323ib and 323ea and selectively set to the conductive state in response to the hold signals HD and/HD. When hold signal HD changes from the L level to the H level and indicates interruption of the supply of external clock signal extCLK, potential storing circuit 323ia converts the input potential Vin on node 323da to a digital signal and stores it, and applies the stored digital signal as an analog signal AN. Transfer gates 323e and 323if are rendered conductive when the hold signal HD changes from the L level to the H level, indicating interruption of the external clock signal extCLK.

Detailed Description Text (109):
The potential storing circuit 323ia includes a resistance element 323ih connected between internal power supply node 300c and node 323ig and having a resistance value

R; a resistance element 323ij connected between nodes 323ig and 323ii and having resistance value R; a resistance element 323im connected between nodes 323ii and 323ik and having resistance value R; a resistance element 323in connected between node 323ik and ground node 300b;a differential amplifying circuit 323ip having a negative input receiving input potential Vin and a positive input receiving the potential (3.multidot.intVCC/4) on node 323ig, for outputting a signal IN1 at the H level when the input signal Vin is lower than node 323ig and otherwise outputting the output signal IN1 at the L level; a differential amplifying circuit 323iq having a negative input receiving input potential Vin and a positive input receiving the potential on node 323ii for outputting a signal IN2 which is at the H level when the input potential Vin is lower than the potential at node 323ii; a differential amplifying circuit 323ir having a negative input receiving the input potential Vin and a positive input receiving the potential (intVCC/4) on node 323ik, for outputting a signal IN3 which attains to the H level when the input potential Vin is lower than the potential on node 323ik; and a latch circuit 323is for latching output signals IN1, IN2 and IN3 from differential amplifying circuits 323ip, 323iq and 323ir in response to transition of data holding signal HD from the L level to the H level, and outputting these as output signals OUT1, OUT2 and OUT3. The output signals IN1, IN2 and IN3 from differential amplifying circuits 323ip, 323iq and 323ir change in digital manner. The latch circuit 323is is formed, for example, by a D type flipflop.

Detailed Description Text (110):
Potential storing circuit 323ia further includes a constant current circuit 323iu connected between internal power supply node 300c and node 323it to which analog signal AN is output, for supplying a constant current i (=intVCC/(4.multidot.R)); resistance elements 323iv1, 323iv2, 323iv3 and 323iv4 connected in series with each other between node 323it and ground node 300b and each having the resistance value R; an n channel MOS transistor 323iw connected at both ends of resistance element 323iv1 and receiving at its gate the signal OUT1 from latch circuit 323if; an n channel MOS transistor 323ix connected parallel to resistance element 323iv2 and receiving at its gate the signal OUT2 from latch circuit 323is; and an n channel MOS transistor 323iy connected parallel to resistance element 323iv3 and receiving at its gate the signal OUT3 from latch circuit 323is.

Detailed Description Text (112):
In potential storing circuit 323ia, if the input potential Vin from node 323da is within a range of ground potential and the potential intVCC/4 at node 323it, the signals IN1, IN2 and IN3 output from differential amplifying circuits 323ip, 323iq and 323ir are set to the H level, H level and H level, respectively. When the input potential Vin is within the range of from the potential (intVCC/4) on node 323ik to the potential (intVCC/2) on node 323ii, the signals IN1, IN2 and IN3 output from differential amplifying circuits 323ib, 323iq and 323ir are set to the H level, H level and L level, respectively. When the input potential Vin is within the range from the potential (intVCC/2) on node 323ii to the potential (3.multidot.intVCC/4) on node 323ig, the signals IN1, IN2 and IN3 output from differential amplifying circuits 323ip, 323iq and 323ir are set to H level, L level, and L level, respectively. When the internal potential Vin is within the range from the potential (3.multidot.intVCC/4) on node 323ig to the internal power supply potential intVCC, the signals IN1, IN2 and IN3 output from differential amplifying circuit 323ip, 323iq and 323ir are set to the L level, L level and L level, respectively.

Detailed Description Text (132):
FIG. 19 shows a structure of a main portion of a semiconductor memory device in accordance with a sixth embodiment of the present invention. In FIG. 19, only the structure of internal clock signal generating circuit 324 included in internal clock signal synchronizing circuit 320 is shown. Other structures are the same as those of any of the first to fifth embodiments. In the structure shown in FIG. 19, a DLL (Delay Locked Loop) circuit is used in place of PLL circuit, to generate internal clock signal intCLK. More specifically, as shown in FIG. 19, instead of the ring oscillator included in internal clock generating circuit 324, a delay circuit receiving external clock signal extCLK is used, as shown in FIG. 19. The internal clock signal generating circuit 324 includes three stages of inverters 324 which receives external clock signal extCLK, delays and inverts it to generate the internal clock signal intCLK. The structure of inverter 324a is the same as that

shown in FIG. 8, and corresponding portions are denoted by the same reference characters.

Detailed Description Text (147):
Differential amplifying circuit 324b includes a p channel current control transistor 324bf connected between internal power supply node 300d for clocks and node 324be and receiving at its gate the p channel current control signal Vp; a p channel MOS transistor 324bg connected between node 324be and output node 324bd and having its gate connected to output node 324bd; a p channel MOS transistor 324bh connected between node 324be and output node 324bc and having its gate connected to output node 324bd; an n channel input transistor 324bj connected between output node 324bd and node 324bi and having its gate connected to input node 324ba; an n channel input transistor 324bk connected between output node 324bc and node 324bi and having its gate connected to input node 324bb; and an n channel current control transistor 324bm connected between node 324bi and ground node 300b and having its gate connected to receive n channel current control signal Vn. The p channel MOS transistors 324bg and 324bh constitute a current mirror circuit.

Detailed Description Text (148):
Differential amplifying circuit (internal clock buffer) 324c receiving complementary output signals of differential amplifying circuit 324b at the last stage serves as an internal clock buffer which differentially amplifies the complementary output signals from differential amplifying circuit 324b at the last stage to generate an internal clock signal intCLK which is set to the H level or the L level. Internal clock buffer 324c includes a p channel MOS transistor 324cb connected between internal power supply node 300c and internal clock signal output node 325 and having its gate connected to node 324ca; a p channel MOS transistor 324cc connected between internal power supply node 300c and node 324c a and having its gate connected to node 324ca; an n channel MOS transistor 324ce connected between internal clock signal output node 325 and node 324cb and having its gate connected to output node 324bd of differential amplifying circuit 324b of the last stage; an n channel MOS transistor 324cf connected between nodes 324ca and 324cd and having its gate connected to output node 324bc of differential amplifying circuit 324b of the last stage; and an n channel MOS transistor 324cg connected between node 324cd and ground node 300b and having its gate connected to internal power supply node 300c. The p channel MOS transistors 324gcc and 324cb constitute a current mirror circuit. The n channel MOS transistor 324cg serving as a current source transistor has its gate connected to internal power supply node 300c, and it has large current drivability. Therefore, internal clock buffer 324c has large operational current, and it drives the internal clock signal intCLK to the H level or to the L level at high speed.

Detailed Description Text (150):
FIG. 22B shows connection between differential amplifying circuit 324b and internal clock buffer 324c shown in FIG. 22A. As shown in FIG. 22B, the positive output signal and the complemental output signal of differential amplifying circuit 324b of the first stage are applied to the positive and negative input nodes of differential amplifying circuit 324b of the second stage. The positive and complemental output signals of differential amplifying circuit 324b of the second stage are applied to the negative and positive input nodes of differential amplifying circuit 324b of the last stage. The positive and complemental output signals from differential amplifying circuit 324b of the last stage are applied to the negative and positive input nodes of differential amplifying circuit 324b of the first stage, as well as to the positive and negative input nodes of internal clock buffer 324c. Each differential amplifying circuit 324b functions as an inversion amplifier, and they constitute a ring oscillator in combination. In this case, differential amplifying circuit 324b has superior amplifying characteristic as compared with an inverter having a common CMOS structure, and amplitude of the positive and negative output signals is made smaller than that between the internal power supply potential Vcc and the ground potential GND (amount of operational current is adjusted by current control signals V.sub.p and Vn). Therefore, the differential amplifying circuits 324b operate at high speed, and output signals change at high speed. Therefore, even when the external clock signal extCLK has a high frequency, internal clock signal intCLK which has its phase synchronized with this high speed external clock signal extCLK can be surely generated.

Detailed Description Text (153):
Differential amplifying circuit 324f includes a p channel current control transistor 324ff connected between internal power supply node 300d for clocks and node 324fe and receiving at its gate the p channel current control signal Vp; a p channel input transistor 324fh connected between nodes 324fe and 324fg and having its gate connected to input node 324fb; a p channel MOS transistor 324fi connected between node 324fe and output node 324fd and having its gate connected to output node 324fd; a p channel MOS transistor 324fj connected between node 324fg and output node 324fc and having its gate connected to output node 324fd; an n channel MOS transistor 324fm connected between output node 324fd and node 324fk and having its gate connected to output node 324fc; an n channel MOS transistor 324fp connected between output node 324fc and node 324fn and having its gate connected to node 324fc; an n channel input transistor 324fq connected between nodes 324fk and 324fn and having its gate connected to input node 324fa; and an n channel current control transistor 324fr connected between node 324fn and ground node 300b and having its gate connected to receive n channel current control signal Vn. The p channel MOS transistors 324fd and 324fj constitute a current mirror circuit, and n channel MOS transistors 324fm and 324fp constitute a current mirror circuit. The current mirror circuits constitute a closed loop, which sets the current flowing through MOS transistors 324fi, 324fj, 324fp and 324fm to the same value.

Detailed Description Text (157):
FIG. 24 shows a still further structure of internal clock signal generating circuit 324. Referring to FIG. 24, each of the differential amplifying circuit 324g connected in a ring includes a p channel current control transistor 324gf connected between internal power supply node 300d for clocks and node 324ge and receiving at its gate p channel current control signal Vp; a p channel MOS transistor 324gh connected between nodes 324ge and 324gg and having its gate connected to output node 324gd; a p channel input transistor 324gi connected between node 324gg and output node 324gd and having its gate connected to input node 324ga; an n channel input transistor 324gk connected between output node 324gb and node 324gd and having its gate connected to input node 324ga; a p channel input transistor 324gm connected between node 324gg and output node 324gc and having its gate connected to input node 324gb; an n channel input transistor 324gn connected between output node 324gc and node 324gj and having its gate connected to input node 324gb, an n channel MOS transistor 324gb connected between nodes 324gj and 324gp and having its gate connected to output node 324gd; and an n channel current control transistor 324gr connected between node 324gp and ground node 300b and having its gate connected to receive n channel current control signal Vn. The p channel input transistor 324gi and n channel input transistor 324gk constitute a CMOS inverter, and p channel input transistor 324gm and n channel input transistor 324gn constitute a CMOS inverter. The operation of the differential amplifying circuit 324g shown in FIG. 24 will be briefly described.

Detailed Description Text (160):
FIG. 25 is a timing chart showing the operation of internal clock signal generating circuit 324 employing the ring oscillator utilizing the differential amplifying circuits shown in FIGS. 22A to 24. FIG. 25 shows output potentials Vout and/Vout of differential amplifying circuit 324b, 324f or 324p of the last stage, as well as internal clock signal intCLK. As shown in (a) of FIG. 25, the complementary output potentials Vout and/Vout do not swing fully between internal power supply potential intVCC and the ground potential GND. However, differential amplifying circuit 324b, 324f or 324g amplifies the applied complementary input signals. As shown in (a) of FIG. 25, in the period from t1 to t2, if the potential Vout becomes higher than the potential/Vout, complementary signals Vout and/Vout are buffered by internal clock buffer 324c, and internal clock signal intCLK is set to the H level of internal power supply potential intVCC. Meanwhile, as shown in (a) of FIG. 25, if the potential Vout becomes lower than the potential /Vout in the period from t2 to t3, the potential difference is amplified by buffer processing, and hence internal clock signal intCLK is set to the L level as shown in (b) of FIG. 25. The speed of operation (speed of response) of differential amplifying circuits 324b, 324f and 324g is determined by the magnitude of the driving current. Therefore, by adjusting operational current (driving current) flowing through these amplifying circuits by current control signals V.sub.p and Vn, the speed of response (speed of operation) of the differential amplifying circuit can be adjusted, and accordingly, the phase

of the internal clock signal intCLK can be adjusted. Here, if the driving current (operational current) decreases, the speed of operation of the differential amplifying circuit decreases, the speed of change in potential at the output node becomes slow, and hence delay time increases.

Detailed Description Text (164):
FIG. 26 shows a structure of a lock in detecting circuit 326. Lock in detecting circuit 326 is included in internal clock signal synchronizing circuit 320. Referring to FIG. 26, lock in detecting circuit 326 includes an extNOR circuit 326a receiving comparing signals/UP and DOWN from phase comparing circuit 321; a p channel MOS transistor 326c connected between external power supply node 300a and node 326b and receiving at its gate an output signal from EXNOR circuit 326a; a resistance element 326d connected between node 326b and ground node 300b;and an inverter 326f for inverting and amplifying signal potential on node 326b and outputting lock in signal LK at output node 326e. The components of lock in detecting circuit 326 all operate using external power supply potential extVCC as one operational power supply potential. When the logic of comparing signal/UP is the same as that of the signal DOWN, EXNOR circuit 326a outputs a signal at the H level, and when these signals have different logics, outputs a signal at the L level. The operation will be described.

Detailed Description Text (165):
When internal clock signal intCLK is not locked in external clock signal extCLK, the period in which comparing signals/UP and DOWN are set to the active level of L and H, respectively, becomes longer. In response, the time in which the output signal from EXNOR circuit 326a is kept at the L level becomes longer, and hence amount of charges for charging node 326b through MOS transistor 326c increases. Therefore, the potential at node 326b attains approximately the level of the external power supply potential extVCC. In this stage, lock in signal LK is set to the L level by inverter 326f.

Detailed Description Text (166):
Meanwhile, as the internal clock signal intCLK comes to be locked in external clock signal extCLK, the period in which comparing signals/UP and DOWN are kept at the active state of L level nd H level, respectively, becomes shorter. In this state, the period in which the output signal of EXNOR circuit 326a is kept at the L level becomes shorter, the amount of charges supplied to node 326d from MOS transistor 326c becomes smaller, and the degree of discharge to the ground node from node 326d through resistance element 326d becomes larger. In this state, the potential at node 326b is set approximately to the ground potential GND level, and lock in signal LK is set to the H level which is at the level of the external power supply potential extVCC, by inverter 326f. Therefore, by the lock in detecting circuit 326 shown in FIG. 26, whether or not the internal clock signal intCLK is locked in external clock signal extCLK can be readily identified. The resistance value of resistance element 326b have only to be set larger than the on resistance of p channel MOS transistor 326c.

Detailed Description Text (167):
FIG. 27 shows a circuit structure of internal power supply potential generating circuit 310a. Internal power supply potential generating circuit 310b for clocks has the same structure as that in FIG. 27. Referring to FIG. 27, internal power supply potential generating circuit 310a includes a constant voltage circuit 311 supplied with current from current supply node 312 for generating an internal power supply potential intVCC at the level of the reference potential Vref at internal power supply node 300c, and a current supplying circuit 316 for supplying current in accordance with a difference between internal power supply potential intVCC and reference potential Vref to current supply node 312. Current supplying circuit 316 includes a current drive transistor 316a connected between external power supply node 300a and current supplying node 312 for supplying current Is from external power supply node 300a to current supply node 312; a gate potential holding circuit 316c for holding gate potential Vg of drive transistor 316a when lock in signal LK is activated; and a current control circuit 316b for adjusting gate potential Vg of drive transistors 316a in accordance with the difference between internal power supply potential intVCC and reference potential Vref.

Detailed Description Text (168):
Current control circuit 316b includes a charge pump circuit 316bg for adjusting gate potential Vg, and a comparing circuit 316bc comparing reference potential Vref with internal power supply potential intVCC for adjusting charge pump operation of charge pump circuit 316bg in accordance with the result of comparison. The comparing circuit 316b includes a differential amplifying circuit 316ba which is activated when lock in signal LK is inactivated, and a differential amplifying circuit 316bb having the same structure as differential amplifying circuit 316ba and which is activated when the lock in signal LK is inactivated. The output potentials Va from differential amplifying circuits 316ba and 316bb are applied to the gates of p channel MOS transistors 316bb and 316bf included in charge pump circuit 316bg.

Detailed Description Text (169):
Differential amplifying circuit 316ba includes a p channel MOS transistor 316bm connected between external power supply node 300a and node 316bj and its gate connected to node 316bk; a p channel MOS transistor 316bn connected between external power supply node 300a and node 316bk and having its gate connected to node 316bk; an n channel MOS transistor 316bg connected between nodes 316bj and 316bp and having its gate connected to receive internal power supply potential intVCC; an n channel MOS transistor 316br connected between nodes 316bb and 316bk and having its gate connected to receive reference potential Vref; and an n channel MOS transistor 316bs connected between node 316bp and ground node 300b and receiving at its gate an inverted signal/LK of lock in signal LK. The p channel MOS transistors 316bn and 316bm constitute a current mirror circuit. The n channel MOS transistor 316bs functions as a current source of differential amplifying circuit 316b. Differential amplifying circuit 316bb also has the same structure as differential amplifying circuit 316ba. Therefore, when the lock in signal LK is set to the active state of L level indicating the state of lock in, the inverted signal /LK is set to the L level, n channel MOS transistor 316bs is rendered non-conductive and differential amplifying circuits 316ba and 316bb are both rendered non-conductive. However, since differential amplifying circuits 316ba and 316bb output Va at H level and L level when inactive, the positions of current source transistors are different.

Detailed Description Text (170):
Holding circuit 316c includes a potential storing circuit 316ca for storing gate potential Vg of current driver transistor 316a when lock in signal LK changes from the L level to the H level; a p channel MOS transistor 316cc connected between external power supply node 300a and node 316cb; a transfer gate 316ce for electrically connecting the gate of current control transistor 316a to node 316cb when lock in signal LK is activated; and a differential amplifying circuit 316cd for comparing the potential on node 316cb with the potential 316ag stored in potential storing circuit 316ca. Potential storing circuit 316ca operates using the external power supply potential extVCC on external power supply node 300a and the ground potential GND on ground node 300e at both operational power supply, converts the gate potential Vg to a digital signal and stores it, and converts the stored digital signal to an analog signal AG for output. The potential storing circuit 316ca has the same structure as potential storing circuit 323ia shown in FIG. 16 except that the external power supply potential extVCC is utilized and that lock in signal LK is used instead of hold signal HD. Therefore, in the potential storing circuit 316ca, the gate potential Vg of current control transistor 316a when the internal clock signal intCLK is locked in external clock signal extCLK is held. Differential amplifying circuit 316cd has the same structure as operational amplifier 323d shown in FIG. 11. Transfer gate 316ce includes a parallel body of an n channel MOS transistor 316ce receiving at its gate the lock in signal LK and a p channel MOS transistor 316cj receiving at its gate the lock in signal/LK.

Detailed Description Text (171):
Circuit 316c further includes a start up circuit 316ch for transmitting a potential of one half the external power supply potential extVCC to the gate of current control transistor 316a. Start up circuit 316ch includes a resistance element 316cg having relatively high resistance, which transmits the potential extVCC/2 applied to node 316cf to the gate of current control transistor 316a. Operational amplifier 316cd receives the potential on node 316cb at its positive input, and receives the analog signal AG at its negative input. Transfer gate 316ce is rendered conductive when lock in signal LK is activated indicating the lock in of the internal clock

signal intCLK.

Detailed Description Text (172):
When the external power supply potential extVCC is applied, a gate potential Vg (=extVCC/2) which is almost the optimum value is transmitted through start up circuit 316ch to the gate of current control drive transistor 316a. Accordingly, the current Is applied to current supply node 312 can be set to the optimal value, and the internal power supply potential intVCC can be set to the prescribed potential level at high speed. When charging/discharging of the gate of current control transistor 316a by charge pump circuit 316bg starts, the charging/discharging current by charge pump circuit 316bg is far larger than the current flowing through resistance elements 316cg having high resistance value. Therefore, start up circuit 316ch hardly contributes to the operation of adjusting the gate potential Vg. By utilizing the internal power supply voltage generating circuit 310a shown in FIG. 27, when internal clock signal intCLK is locked in and the internal circuit operation stabilized, the constant current IS can be supplied stably and the internal power supply potential intVCC can be maintained at the prescribed potential level accordingly, by adjusting the gate potential Vg of current control transistor 316a at a constant potential level when the internal clock signal intCLK is locked in.

Detailed Description Text (173):
Further, in the internal power supply voltage generating circuit 310b for clocks, when the internal clock signal intCLK is locked in, the amount of current consumption does not change, since the operation of the internal clock signal synchronizing circuit is stabilized, the amount of current consumption is constant, and hence by supplying optimal current Is through current control transistor 316a, the internal power supply potential intVCC applied to internal power supply node for clocks can be maintained at the constant potential level.

Detailed Description Text (174):
At this time (when locked in), the output potential Va of differential amplifying circuit 316ba is set to the H level, and output potential Va of differential amplifying circuit 316bb is set to the L level. Therefore, in the differential amplifying circuit 316bb, current source transistor 316bs is formed by a p channel MOS transistor receiving at its gate the lock in signal, and it is provided between external power supply node 300a and p channel MOS transistors constituting the current mirror circuit. The differential amplifying circuits 316ba and 316bb have the same circuit structure except the position of the current source transistor and the polarity of the lock in signal. Therefore, when the lock signal LK is activated, charge pump operation of charge pump circuit 316bg is inhibited, and gate potential Vg of current control transistor 316a is held at the potential level at the time of locked in.

Detailed Description Text (175):
FIG. 28 shows a modification of internal power supply voltage generating circuit 310b for clocks. In the structure shown in FIG. 28, hold signal HD is used instead of the lock signal LK. The hold signal HD is set to the H level when supply of the internal clock signal extCLK is stopped. Except this point, the structure is the same as that shown in FIG. 27, and corresponding portions are denoted by the same reference characters. By using the structure shown in FIG. 28, when the supply of the external clock signal extCLK is stopped, the gate potential Vg of current control transistor 316a is held by potential holding circuit 316c. Therefore, when the supply of the external clock signal extCLK is resumed, the current Is applied to current supply node 312 can be set to the optimal value at high speed.

Detailed Description Text (177):
FIG. 29 shows a structure of a main portion of a semiconductor memory device in accordance with a ninth embodiment of the present invention. FIG. 29 shows the structures of internal power supply potential generating circuits 310a and 310b.Other structures are the same as the embodiments above. The internal power supply potential generating circuits 310a, and 310b shown in FIG. 29 differ from the above embodiments in the following points. In constant voltage circuit 311, an analog current driver transistor 311a connected between external power supply node 300a and internal power supply node 300c and receiving at its gate an analog driver

control signal DRVA from differential amplifying circuit 314 is provided. The driver control signal DRVA is a signal obtained by amplifying a potential difference between internal power supply potential intVCC and the reference potential Vref from reference potential generating circuit 313, and it is an analog signal. The driver transistor 311a is rendered conductive when internal power supply potential intVCC is lower than the reference potential Vref.

Detailed Description Text (178):
Further, in differential amplifying circuit 314, a p channel MOS transistor 314j connected between external power supply node 300a and node 314i and having its gate connected to node 314b, and an n channel MOS transistor 314k connected between nodes 314i and 314d and having its gate connected to receive reference potential Vref are provided. The p channel MOS transistor 314j and p channel MOS transistor 314f constitute a current mirror circuit. Between the output node 314i of differential amplifying circuit 314 and the gate of driver transistor 315, a buffer circuit 311b is provided. When internal power supply potential intVCC becomes lower than the reference potential Vref by about Vref/10, buffer circuit 311b sets the driver control signal DRVD to extVCC-2.vertline.Vthp.vertline., and otherwise sets it to the level of external power supply potential extVCC. Here, Vthp represents the threshold voltage of p channel MOS transistor. More specifically, buffer circuit 311b has a function of converting the analog signal DRVA output from the differential amplifying circuit 314 to digital driver control signal DRVD. Therefore, driver transistor 315 is rendered conductive when internal power supply potential intVCC lowers by Vref/10 or more from reference potential Vref, and otherwise it is rendered non-conductive, and it is digitally turned on/off. The internal power supply potential generating circuit in which digital control driver transistor 315 and analog control driver transistor 311a coexist is referred to as a mixed mode internal power supply potential generating circuit.

Detailed Description Text (179):
In current supplying circuit 316, charge pump circuit 316bj for adjusting gate potential Vg of current control transistor 316 includes an n channel MOS transistor 316bx and a p channel MOS transistor 316bw serving as a constant current source. The p channel MOS transistor 316bw is connected between p channel MOS transistor 316be for charging and internal power supply node 300a, and has its gate connected to receive ground potential GND. The n channel MOS transistor 316bx is connected between n channel MOS transistor 316bf for discharging and ground node 300b,and has its gate connected to receive external power supply potential extVCC. The analog charge pump circuit 316bg increases the gate potential Vg by charging the gate of current control transistor 316a when the internal power supply potential intVCC is higher than the reference potential Vref, in accordance with the analog output potential Va output from differential amplifying circuit 316bc, and otherwise, it lowers the gate potential Vg by discharging the gate of current control transistor 316a.

Detailed Description Text (180):
Current supplying circuit 316 further includes a digital converting circuit 316bt for converting the analog output potential Va from comparing circuit 316bc to output potentials DVu and DVd which change in digital manner, and a digital charge pump circuit 316bd for adjusting gate potential Vg of current control transistor 316a in accordance with output potentials DVu and DVd from digital converting circuit 316bt. Digital converting circuit 316bt includes a buffer circuit 316bu receiving the output potential Va from comparing circuit 316bc for outputting a digital output potential DVu, and an inverter buffer circuit 316bv receiving analog output potential Va from comparing circuit 316bc for generating a digital output potential DVd. A circuit 316bu sets the digital output potential DVu to the level of the ground potential GND when the potential level of the analog output potential Va from comparing circuit 316bc corresponds to the state in which internal power supply potential intVCC becomes higher by at least Vref/10 than the reference potential Vref, and otherwise it sets the digital output potential DVu to the level of the external power supply potential extVCC. Inverter buffer circuit 316bv sets the digital output potential DVd to the level of the external power supply potential extVCC when the analog output potential Va from comparing circuit 316bc corresponds to the state in which the internal power supply potential intVCC becomes lower by at least Vref/10 than the reference potential Vref, and otherwise sets the digital

output potential DVd to the level of the ground potential GND. The input logic threshold voltages of these buffer circuits 316bu and 316bv are adjusted to implement such logic operations.

Detailed Description Text (181):
More specifically, as shown in FIG. 30, when the internal power supply potential intVCC lowers by Vref/10 or more from the reference potential Vref at time t0, in accordance with the potential level of analog output potential Va, the digital output potential DVd is set to the level of the external power supply potential extVCC. The digital output potential DVd holds the potential level of the external power supply potential extVCC until the time t1, while the internal power supply potential intVCC is lower by at least Vref/10 than the reference potential Vref. After the time point t1, when the difference between internal power supply potential intVCC and reference potential Vref becomes smaller than Vref/10, the digital output potential DVd is set to the level of the ground potential GND. Meanwhile, at time t2, if the internal power supply potential intVCC becomes higher than the reference potential Vref by at least Vref/10, the digital output potential DVu is set to the level of the ground potential GND. At time t3, when the difference between the internal power supply potential Vcc and reference potential Vref becomes smaller than Vref/10, the digital output potential DVu is set to the level of the external power supply potential extVCC.

Detailed Description Text (182):
Digital charge pump circuit 316d includes a p channel MOS transistor 316db receiving the digital output potential DVu from buffer circuit 316bu for charging the gate of current control transistor 316a; a p channel MOS transistor 316da connected between p channel MOS transistor 316db and external power supply node 300a and having its gate connected to receive ground potential GND and functioning as a constant current source; an n channel MOS transistor 316dc receiving at its gate the digital output potential DVd from inverter buffer circuit 316bv for discharging the gate of current control transistor 316a; and an n channel MOS transistor 316dd connected between n channel MOS transistor 316dc and ground node 300b and having its gate connected to receive external power supply potential extVCC and functioning as a constant current source.

Detailed Description Text (183):
The buffer circuit 311b which applies digital control signal DRVD to the gate of current driver transistor 315 includes diode connected p channel MOS transistors 311ba, 311bb and 311bc connected in series between external power supply node 300a and node 311bx; an n channel MOS transistor 311bd connected between node 311bx and ground node 300b and having its gate connected to external power supply node 300a, functioning as a resistance element, a p channel MOS transistor 311ba and an n channel MOS transistor 311bf connected between external power supply node 300a and node 311bi for constituting a CMOS inverter which inverts and amplifies the output signal from differential amplifying circuit 314; a p channel MOS transistor 311bg and an n channel MOS transistor 311bh connected between external power supply mode 300a and node 311bi for constituting a CMOS inverter for inverting and amplifying an output signal from the CMOS inverter of the first stage; and a p channel MOS transistor 311bj connected between node 311bi and ground node 300b and having its gate connected to node 311bx.

Detailed Description Text (185):
The operation when the internal power supply potential intVCC is lower than the reference potential Vref generated from reference potential generating circuit 313 will be described. In this case, as the internal power supply potential intVCC lowers, the driver control signal DRVA output from differential amplifying circuit 314 lowers from a potential near the boundary between conduction/non-conduction of analog control drive transistor 311a gradually to the ground potential. In response, the conductance of analog control drive transistor 311a increases proportionally, and accordingly, the current flowing from external power supply node 300a to internal power supply node 300c through analog control drive transistor 311a also increases.

Detailed Description Text (186):
Until the internal power supply potential intVCC lowers by at least Vref/10 from the

reference potential Vref, the potential at output node 314i of differential amplifying circuit 314 is higher than the logical threshold of the inverter constituted by transistors 311be and 311bf in buffer circuit 311b. Therefore, the digital driver control signal DRVD output from buffer circuit 311b is set to the level of the external power supply potential extVCC, and digital control drive transistor 315 is rendered non-conductive. Therefore, even when the internal power supply potential intVCC lowers from reference potential Vref, current is supplied to the internal power supply node 300c only by the analog control drive transistor 311a. Therefore, if the internal power supply potential intVCC increases to the reference potential Vref in this state, digital control driver transistor 315 is kept non-conductive.

Detailed Description Text (187):
When the amount of consumption of internal power supply potential intVCC is larger than the current supplied from analog control drive transistor 311a, the internal power supply potential intVCC is continuously lowered. When the internal power supply potential intVCC becomes lower than the reference potential Vref by at least Vref/10, the potential at output node 314i of differential amplifying circuit 314 becomes lower than the logical threshold value of the inverter constituted by transistors 311be and 311bf of buffer circuit 311b, and the digital driver control signal DRVD output from buffer circuit 311b is set to the potential applied to node 311bi, that is, extVCC-2.vertline.Vthp.vertline.. In response, digital control drive transistor 315 is rendered conductive, and as a large current is supplied to internal power supply node 300c through the digital control drive transistor 315 which has wider channel width than analog control drive transistor 311b, that is, having larger current drivability, the internal power supply potential intVCC can be returned quickly to the reference potential Vref. By controlling the potential level of the lower limit of the signal DRVD, generation of an overshoot is prevented, as a large current is suppressed due to the limitation of conductance of the digital drive transistor.

Detailed Description Text (188):
When the internal power supply potential intVCC becomes higher than the reference potential Vref, the analog driver control signal DRVA increases from the potential at the boundary between conduction/non-conduction of analog control drive transistor 311a, and analog control drive transistor 311a is rendered non-conductive. Since the potential at output 314i from differential amplifying circuit 314 is also higher than the logical threshold voltage of the inverter in buffer circuit 311b, digital driver control signal DRVD attains to the level of the external power supply potential extVCC, and digital control drive transistor 315 is rendered non-conductive. In this state, when the internal power supply potential intVCC is used by the internal circuitry, the internal power supply potential intVCC gradually lowers as it is consumed.

Detailed Description Text (189):
When large amount of current is supplied to internal power supply node 300c through digital control drive transistor 315, there will be a large overshoot of internal power supply potential intVCC, and if the current amount is small, there will be a large undershoot. In order to optimize the overshoot and the undershoot, current drivability of current control transistor 316a is controlled by current supplying circuit 316, in accordance with the difference between internal power supply potential intVCC and the reference potential Vref. In the current control circuit 316, when the internal power supply potential intVCC becomes lower than the reference potential Vref, the analog output potential Va output from comparing circuit 316bc increases, the p channel MOS transistor 316be and n channel MOS transistor 316bf in analog charge pump circuit 316bg are rendered nonconductive and conductive, respectively. In response, the gate potential Vg of current control transistor 316a lowers, and current drivability of the current control transistor 316a increases.

Detailed Description Text (190):
If the undershoot of external power supply potential intVCC increases and internal power supply potential intVCC becomes lower than the reference potential Vref by Vref/10 or more, the analog output potential Va output from comparing circuit 316c becomes higher than the logical threshold voltage of inverter buffer circuit 316bv

in digital converting circuit 316bt, and the digital output potential DVd from the inverter buffer circuit 316bv is set to the level of the external power supply potential extVCC. Meanwhile, analog output potential Va is higher than the logical threshold voltage of buffer circuit 316bu (which is lower than the logical threshold voltage of buffer circuit 316bv), the digital output potential DVu from buffer circuit 316bu attains to the external power supply potential extVCC, and p channel MOS transistor 316db and n channel MOS transistor 316dc in digital charge pump circuit 316d are set to the nonconductive state and conductive state, respectively. Consequently, the gate of current control transistor 316a is discharged rapidly through n channel MOS transistor 316dc having a large channel width, the current drivability of current control transistor 316a increases rapidly, and a large current is applied from external power supply node 300a to current driver transistor 315.

Detailed Description Text (191):
When the overshoot of internal power supply potential intVCC is large and internal power supply potential intVCC is increased from reference potential Vref by at least Vref/10, the analog output potential Va output from comparing circuit 316bc becomes lower than the logical threshold voltage of buffer circuit 316bu of digital converting circuit 316bt, and the digital output potential DVu from buffer circuit 316bu is set to the level of the ground potential GND. Meanwhile, the analog output potential Va from comparing circuit 316bc is lower than the logical threshold voltage (which is set higher than the logical threshold voltage of buffer circuit 316bu) of inverter buffer circuit 316bv, and hence the output potential DVd from inverter buffer circuit 361bv is also set to the level of the ground potential GND. Consequently, the p channel MOS transistor 316db and n channel MOS transistor 316dc in digital charge pump circuit 316d are rendered conductive and non-conductive, respectively, the gate of the current control transistor 316a is quickly charged through p channel MOS transistor 316db having wide channel width, and the current drivability of current control transistor 316 lowers quickly. Consequently, the current applied from external power supply node 300a to current driver transistor 315 is reduced quickly and overshoot is suppressed.

Detailed Description Text (192):
As described above, when the mixed mode internal power supply potential generating circuit is used, when the potential difference between internal power supply potential intVCC and reference potential Vref is, both the analog control drive transistor 311a and digital control drive transistor 315a are rendered conductive, and internal power supply potential intVCC is quickly returned to the reference potential Vref. Meanwhile, if the potential difference between internal power supply potential intVCC and reference potential Vref is small, only the analog control drive transistor 311a is rendered conductive, and the internal power supply potential intVCC is precisely returned to the reference potential Vref. Therefore, the internal power supply potential intVCC can be set at high speed and precisely to the reference potential vref.

Detailed Description Text (193):
Further, since analog charge pump circuit 316bg and digital charge pump circuit 316d are provided in current supplying circuit 316, when the internal power supply potential intVCC is in the range from Vref-Vref/10 to Vref+Vref/10, gate of the current control transistor 316a is charged/discharged only by the analog charge pump circuit 316bg, and when it is out of this range, the gate of the current control transistor 316a is charged/discharged by both the analog charge pump circuit 316bg and digital charge pump circuit 316d. Therefore, when the internal power supply potential intVCC largely deviates from the reference potential Vref, the gate of the current control transistor 316a is charged/discharged by two charge pump circuits 316bg and 316d, and therefore the gate potential quickly comes near to the optimal value (rough adjustment of gate potential), and if the internal power supply potential intVCC is close to the reference potential Vref, the gate of current control transistor 316a is charged/discharged only by the analog charge pump circuit 316bg, and therefore the gate potential can be approached to the optimal value precisely (fine adjustment of gate potential). Therefore, the gate potential of current control transistor 316a can be set to the optimal value at high speed and precisely. The buffer 311b may be operated in digital manner, in accordance with the magnitude of intVCC and Vref. The supply current is surely adjusted by current

supplying circuit 316.

Detailed Description Text (197):
Further, in current supplying circuit 316, comparing circuit 316bc is inactivated when the lock in signal LK is activated. The comparing circuit 316bc outputs a signal at the H level when inactivated, that is, when the internal clock signal intCLK is locked in the external clock signal extCLK. In this case, the output potential DVu of digital converting circuit 316bt is set to the level of the external power supply potential extCLK, and digital output potential DVd is set to the level of the ground potential GND. Therefore, in the digital charge pump circuit 316d and analog charge pump circuit 316bg, p channel MOS transistors 316db and 316be as well as n channel MOS transistors 316dc and 316bf are all rendered non-conductive, and charging/discharging operation of gate potential Vg of current control transistor 316a is stopped. In holding circuit 316c, the gate potential Vg is held at the potential level at the time of lock in. At the time of lock in, internal clock signal synchronizing circuit 320 hardly performs operation for adjusting frequency/phase of internal clock signal intCLK, and internal clock signal intCLK is generated stably. Therefore, in this case, the current consumption is almost constant, and by holding the gate potential Vg of current control transistor 316a at the time of lock in, a current corresponding to the constant consumed current can be supplied to the internal power supply node 300c. More specifically, at the lock in operation, the amount of current supplied through digital control drive transistor 315 to internal power supply node 300c can be maintained at the optimal value. Consequently, the internal power supply potential intVCC with respect to the internal clock synchronizing circuit 320 can be maintained at a constant potential level, and hence internal clock signal intCLK can be generated stably.

Detailed Description Text (198):
Further, the potential holding circuit 316c includes a start up circuit 316ch, as shown in FIG. 28. Therefore, when the power is turned on, the gate potential Vg of current control transistor 316a is set to the extVCC/2, which is close to the optimal value, and hence the amount of current supplied by current control transistor 316a can be set to the optimal state at high speed after power on. Therefore, the internal power supply potential intVCC can be set to the prescribed level of reference potential Vref at high speed.

Detailed Description Text (200):
FIG. 32 shows a structure of a main portion of a semiconductor memory device in accordance with an eleventh embodiment of the present invention. In FIG. 32, the structures of internal power supply potential generating circuits 310a and 310b are shown. Other structures are the same as any of Embodiments 1 to 10 above, and corresponding portions are denoted by the same reference characters and detailed description thereof is not repeated. In the eleventh embodiment, the internal power supply potential intVCC is set to the potential level lower by the threshold voltage Vthn of n channel MOS transistor than reference potential Vref.

Detailed Description Text (201):
More specifically, the constant voltage circuit 311 includes an n channel MOS transistor 311c connected between external power supply nodes 300a and 300c and receiving at its gate the reference potential Vref; and an n channel MOS transistor 317 connected between external power supply node 300a and current control transistor 316a and receiving at its gate the reference potential Vref. Current control transistor 316a directly supplies current to internal power supply node 300c.

Detailed Description Text (202):
In current control circuit 316, an n channel MOS transistor 316bj for transmitting reference potential Vref from reference potential generating circuit 313 to comparing circuit 316bc in the source follower mode is provided. The n channel MOS transistor 316bj has one conduction node (drain) connected to external power supply node 300a, and another conduction node (source) coupled to a positive input of differential amplifying circuits 316ba and 316bb included in comparing circuit 316bc. Drive transistors (n channel MOS transistors) 311c and 317 have a threshold voltage Vthn, and have the same channel length. However, in order to increase current drivability, drive transistor 317 has wider channel width than drive transistor 311c. The threshold voltage of n channel MOS transistor 316bj is also the

same Vthn as drive transistors 311c and 317. Transistors 311c, 316bj and 317 have their gate potentials lower than the drain, the transistors operate in the source follower mode, and transmit the potential which is lower by the threshold voltage than the potential applied to their gates to their sources. Therefore, transistor 311c is rendered conductive when the internal power supply potential intVCC on internal power supply node 300c becomes lower than Vref-Vthn, and transmits the current to internal power supply node 300c. Meanwhile, if the internal power supply potential intVCC increases to be higher than the potential Vref-Vthn, drive transistor 311c is rendered non-conductive (since the gate-source potential difference becomes smaller than the threshold voltage thereof). Drive transistor 317 serves as a current supply source for the current control transistor 310a. When the internal power supply potential intVCC increases to be higher than the potential Vref-Vthn, current control transistor 316a is rendered non-conductive, and accordingly, driver transistor 317 is also rendered non-conductive. Meanwhile, if the internal power supply potential intVCC becomes not higher than Vref-Vthn, the gate potential Vg of current control transistor 316a lowers, current control transistor 316a is rendered conductive, and accordingly, drive transistor 317 is rendered conductive as the source potential lowers, so that it supplies current to current control transistor 316a. Therefore, the drive transistor 317 is also rendered conductive/non-conductive in accordance with the potential level of internal power supply potential intVCC.

Detailed Description Text (203):
Comparing circuit 316bc compares the potential Vref-Vthn with internal power supply potential intVCC through n channel MOS transistor 316bj. Therefore, operations of digital charge pump circuit 316d and analog charge pump circuit 316bg are controlled in accordance with the difference between internal power supply potential intVCC and potential Vref-Vthn, and the gate potential Vg of current control transistor 316a is controlled accordingly. When the undershoot of internal power supply potential intVCC is small, current is supplied through drive transistor 311c, and also current is supplied through analog charge pump circuit 316bg and current control transistor 316a. If the undershoot of internal power supply potential intVCC is, the gate potential Vg of current control transistor 316a is controlled by analog charge pump circuit 316bg and digital charge pump circuit 316d, and large current is supplied to internal power supply node 300c. Therefore, by using the structure shown in FIG. 32 also, the internal power supply potential intVCC can be stably held at the constant potential level of Vref-Vthn. In accordance with the structure shown in FIG. 32, in the constant voltage circuit 311, the difference amplifying circuit for comparing internal power supply potential intVCC with reference potential Vref is not necessary, and hence the area of occupation by the circuits can be reduced.

Detailed Description Text (206):
A clock synchronous type SRAM has been described as an example of a semiconductor memory device in the embodiments above. However, the present invention is also applicable to a synchronized type semiconductor memory device such as a synchronous DRAM which operates in synchronization with an externally applied clock signal. Further, the structure of the internal power supply potential generating circuit itself may be applied to a standard DRAM, as an internal voltage lowering circuit for generating an internal power supply potential intVCC from the external power supply potential extVCC. Further, in the internal power supply potential generating circuit, the driver transistor for supplying current constituted by a p channel MOS transistor may be replaced by a pnp bipolar transistor. Further, the driver transistor for supplying current constituted by an n channel MOS transistor may be replaced by an npn bipolar transistor.

CLAIMS:

1. A semiconductor device, comprising:

a difference adjusting circuit for detecting a difference in at least one of phase and frequency between an incoming first signal and a second signal, and for generating a control signal for making the difference smaller;

a differential amplifying circuit for differentially amplifying said control signal from said difference adjusting circuit and a feedback potential;

an internal clock signal generating circuit for generating said second signal responsive to an operational current;

adjusting means for adjusting the operational current in accordance with an output signal from said differential amplifying circuit;

a current supplying element for generating a current in accordance with the output signal from said differential amplifying circuit;

a variable resistance element for converting the current generated by said current supplying element to a voltage signal to generate said feedback potential; and

a resistance value switching circuit for switching a resistance value of said variable resistance element, wherein

said variable resistance element is an insulated gate type field effect transistor, and

said resistance value switching circuit includes means for reducing the resistance value of said variable resistance element when a power is applied to said semiconductor device.

2. A semiconductor devices, comprising:

a difference adjusting circuit for detecting a difference in at least one of phase and frequency between an incoming first signal and a second signal, and for generating a control signal for making the difference smaller;

a differential amplifying circuit for differentially amplifying said control signal from said difference adjusting circuit and a feedback potential;

an internal clock signal generating circuit for generating said second signal responsive to an operational current;

adjusting means for adjusting the operational current in accordance with an output signal from said differential amplifying circuit;

a current supplying element for generating a current in accordance with the output signal from said differential amplifying circuit;

a variable resistance element for converting the current generated by said current supplying element to a voltage signal to generate said feedback potential; and

a resistance value switching circuit for switching a resistance value of said variable resistance element, wherein

said difference adjusting circuit includes,

a comparing circuit coupled to receive said first and second signals, for outputting first and second comparing signals in accordance with a difference of at least one of phase and frequency of the received first and second signals, and

a charge pump circuit having input nodes receiving said first and second comparing signals, and a charging/discharging node, for charging said charging/discharging node in accordance with said first comparing signal and for discharging said charging/discharging node in accordance with said second comparing signal; and

said resistance value switching circuit includes a resistance control circuit for adjusting the resistance value of said variable resistance element in accordance with coincidence/non-coincidence of logics of said first and second comparing signals.

3. A semiconductor devices, comprising:

a difference adjusting circuit for detecting a difference in at least one of phase and frequency between an incoming first signal and a second signal, and for generating a control signal for making the difference smaller;

a differential amplifying circuit for differentially amplifying said control signal from said difference adjusting circuit and a feedback potential;

an internal clock signal generating circuit for generating said second signal responsive to an operational current;

adjusting means for adjusting the operational current in accordance with an output signal from said differential amplifying circuit;

a current supplying element for generating a current in accordance with the output signal from said differential amplifying circuit;

a resistance element for converting the current generated by said current supplying element to a voltage signal to generate said feedback potential; and

a transfer gate provided between an output portion of said difference adjusting circuit and an input portion of said differential amplifying circuit and rendered non-conductive when supply of said first signal is stopped.

4. A semiconductor device, comprising:

a difference adjusting circuit for detecting a difference in at least one of phase and frequency between an incoming first signal and a second signal, and for generating a control signal for making the difference smaller;

a differential amplifying circuit for differentially amplifying said control signal from said difference adjusting circuit and a feedback potential;

an internal clock signal generating circuit for generating said second signal responsive to an operational current;

adjusting means for adjusting the operational current in accordance with an output signal from said differential amplifying circuit;

a current supplying element for generating a current in accordance with the output signal from said differential amplifying circuit;

a resistance element for converting the current generated by said current supplying element to a voltage signal to generate said feedback potential; and

a transfer gate coupled between said current supplying element and said resistance element and rendered non-conductive when supply of said first signal is stopped.

5. A semiconductor device, comprising:

a difference adjusting circuit for detecting a difference in at least one of phase and frequency between an incoming first signal and a second signal, and for generating a control signal for making the difference smaller;

a differential amplifying circuit for differentially amplifying said control signal from said difference adjusting circuit and a feedback potential;

an internal clock signal generating circuit for generating said second signal responsive to an operational current;

adjusting means for adjusting the operational current in accordance with an output signal from said differential amplifying circuit;

a current supplying element for generating a current in accordance with the output signal from said differential amplifying circuit;

a resistance element for converting the current generated by said current supplying element to a voltage signal to generate said feedback potential; and

potential holding circuit coupled to a first input portion, receiving the control signal from said difference adjusting circuits, of said differential amplifying circuit for holding a potential applied to said first input portion of said differential amplifying circuit when supply of said first signal is stopped.

6. The semiconductor device according to claim 5, wherein

said potential holding circuit includes a potential storing circuit activated in response to no supply of said first signal, for converting and latching the potential at said first input portion of said differential amplifying circuit to a digital signal, and converting the latched signal to an analog signal for output, a second differential amplifying circuit having a first input node receiving said analog signal and a second input node receiving a potential at a first node, for differentially amplifying potentials at said first and second input nodes, and a holding current supplying element for supplying current from a first power supply node to said first node in accordance with an output signal from said second differential amplifying circuit.

7. A semiconductor device, comprising:

a differential adjusting circuit for detecting a difference in at least one of phase and frequency between an incoming first signal and a second signal, and for generating a control signal for making the difference smaller;

a differential amplifying circuit for differentially amplifying said control signal from said difference adjusting circuit and a feedback potential;

an internal clock signal generating circuit for generating said second signal responsive to an operational current;

adjusting means for adjusting the operational current in accordance with an output signal from said differential amplifying circuit;

a current supplying element for generating a current in accordance with the output signal from said differential amplifying circuit;

a resistance element for converting the current generated by said current supplying element to a voltage signal to generate said feedback potential;

a reference potential generating circuits, coupled to receive a power supply potential, for generating a reference potential not dependent on fluctuation of said power supply potential;

a drive transistor and a current control transistor connected in series to each other between a power supply node to which said power supply potential is supplied and an internal power supply node;

an adjusting circuit for adjusting a gate potential of said drive transistor in accordance with a difference between a potential on said internal power supply node and said reference potential; and

a current control circuit for adjusting a gate potential of said current control transistor in accordance with a difference between said reference potential and an internal power supply potential on said internal power supply node; wherein

the internal power supply potential on said internal power supply node is supplied as one operational power supply potential of said internal clock signal generating circuit.

12. The semiconductor device according to claim 7, wherein

said current control transistor is a p channel insulated gate type field effect

transistor;

said current control circuit includes an analog charge pump circuit for charging the gate of said current control transistor when said internal power supply potential is higher than said reference potential, and otherwise for discharging the gate of said current control transistor, and

a digital charge pump circuit for charging the gate of said current control transistor when said internal power supply potential is higher by at least a prescribed value than said reference potential, and for discharging the gate of said current control transistor when said internal power supply potential is lower by at least a prescribed value, than said reference potential.

13. A semiconductor device, comprising:

difference adjusting circuit for detecting a difference in at least one of phase and frequency between an incoming first signal and a second signal, and for generating a control signal for making the difference smaller;

a differential amplifying circuit for differentially amplifying said control signal from said difference adjusting circuit and a feedback potential;

an internal clock signal generating circuit for generating said second signal responsive to an operational current;

adjusting means for adjusting the operational current in accordance with an output signal from said differential amplifying circuit;

a current supplying element for generating a current in accordance with the output signal from said differential amplifying circuit;

a resistance element for converting the current generated by said current supplying element to a voltage signal to generate said feedback potential;

an analog current driver connected between a first power supply node and an internal power supply node, and having its conductance increased when a potential on said internal power supply node is lower than a prescribed potential, in accordance with the difference in potential therebetween;

a current control transistor and a digital drive transistor connected in series to each other between said first power supply node and said internal power supply node;

a current control circuit for adjusting a gate potential of said current control transistor in accordance with a difference between the potential on said internal power supply node and said prescribed potential; and

a digital control circuit for rendering conductive/non-conductive said digital drive transistor in a digital manner in accordance with the difference between the potential on said internal power supply node and said prescribed potential; wherein

the potential on said internal power supply node is supplied as one operational power supply potential of said internal clock signal generating circuit.

14. The semiconductor device according to claim 7, wherein

said current control transistor is a p channel MOS transistor, and

said current control circuit includes

an analog charge pump circuit for charging the gate of said current control transistor when the internal power supply potential on said internal power supply node is higher than said reference potential and for discharging the gate of said current control transistor when the internal power supply potential is lower than the reference potential, and

a digital charge pump circuit for charging the gate of said current control transistor when said internal power supply potential is higher by a prescribed value than said reference potential and for discharging the gate of said current control transistor when said internal power supply potential is lower than said reference potential.

16. A semiconductor device, comprising:

a comparing circuit having first and second clock signal input nodes, for detecting a difference in at least one of phase and frequency of first and second clock signals applied to said first and second clock signal input nodes and for outputting first and second comparing signals for decreasing said difference;

a charge pump circuit receiving said first and second comparing signals for charging a charging/discharging node when said first comparing signal is active, and for discharging said charging/discharging node when said second comparing signal is active;

a current control circuit including a transfer gate connected between said charging/discharging node and a first node, receiving a hold designating signal and rendered non-conductive when said hold designating signal is active, for outputting a current control signal in accordance with the potential at said first node; and

an internal clock signal generating circuit of which operational current is adjusted in accordance with said current control signal, for outputting said second clock signal, wherein

said current control circuit further includes a potential holding circuit for holding the potential at said first node when said hold designating signal is at the active state.

17. A semiconductor device, comprising

a comparing circuit having first and second clock signal input nodes, for outputting first and second comparing signals in accordance with a difference in at least one of phase and frequency of first and second clock signals applied to said first and second clock signal input nodes for reducing said difference;

a charge pump circuit receiving said first and second comparing signals, charging a charging/discharging node when said first comparing signal is active, and for discharging said charging/discharging node when said second comparing signal is active;

a current control circuit for outputting a current control signal in accordance with a potential on said charging/discharging node;

an odd number of amplifying circuits connected in a ring, each having driving current controlled in accordance with said current control signal, and each inverting and amplifying complementary input signals and outputting complementary output signals; and

a clock buffer for buffering an output from the amplifying circuit of the last stage of the amplifying circuits in the ring for outputting said second clock signal, wherein

said current control circuit includes a control stage for outputting a p channel current control signal and an n channel current control signal for supplying a same amount of current in accordance with the potential at said charging/discharging node; and

each said amplifying circuit includes

a p channel current control transistor coupled between a power supply node and a first node and receiving at its gate said p channel current control signal,

a first p channel MOS transistor coupled between said first node and a first output node and having its gate coupled to said first output node,

a first input p channel MOS transistor coupled between said first node and a second node and receiving at its gate one of said complementary input signals,

a second p channel MOS transistor coupled between said second node and a second output node and having its gate coupled to said first output node,

a first n channel MOS transistor coupled between said firs output node and a third node and having its gate coupled to said second output node,

a second n channel MOS transistor coupled between said third node and a fourth node and receiving another of said complementary input signals,

a third n channel MOS transistor coupled between said second output node and said fourth node and having its gate coupled to said second output node, and

an n channel current control MOS transistor connected between said fourth node and a ground node and receiving at its gate said n channel current control signal.

18. A semiconductor device, comprising:

a comparing circuit having first and second clock signal input nodes, for outputting first and second comparing signals in accordance with a difference in at least one of phase and frequency of first and second clock signals applied to said first and second clock signal input nodes for reducing said difference;

a charge pump circuit receiving said first and second comparing signals, charging a charging/discharging node when said first comparing signal is active, and for discharging said charging/discharging node when said second comparing signal is active;

a current control circuit for outputting a current control signal in accordance with a potential on said charging/discharging node;

an odd number of amplifying circuits connected in a ring, each having driving current controlled in accordance with said current control signal, and each inverting and amplifying complementary input signals and outputting complementary output signals; and

a clock buffer for buffering an output from the amplifying circuit of the last stage of the amplifying circuits in the ring for outputting said second clock signal, wherein

said current control circuit includes means for generating a p channel current control signal and an n channel current control signal for supplying a same amount of current in accordance with the potential on said charging/discharging node; and

each said amplifying circuit includes

a current control p channel MOS transistor coupled between a power supply node and a first node and receiving at its gate said p channel current control signal,

a first p channel MOS transistor coupled between said first node and a second node and having its gate coupled to a first output node,

a second p channel MOS transistor coupled between said second node and said first output node and receiving at its gate one of said complementary input signals,

a first n channel MOS transistor coupled between said first output node and a third node and receiving at its gate said one of said complementary input signals,

a third p channel MOS transistor coupled between said second node and a second

output node and receiving at its gate the other of said complementary input signals,

a second n channel MOS transistor coupled between said second output node and said third node and receiving at its gate said other of said complementary input signals,

a third n channel MOS transistor coupled between said third node and a fourth node and having its gate coupled to said first output node, and

a current control n channel MOS transistor coupled between said fourth node and a ground node and receiving at its gate said n channel current control signal.

19. A semiconductor device, comprising:

a reference potential generating circuit receiving a power supply potential for generating a reference potential not dependent on the power supply potential;

a drive transistor and a current control transistor connected in series to each other between a power supply node to which the power supply potential is supplied and an internal power supply node; and

a current control circuit coupled to receive said reference potential and an internal potential on said internal power supply node, for controlling control electrode potentials of said drive transistor and said current control transistor such that a current in accordance with a difference between said reference potential and said internal potential flows through said drive transistor and said current control transistor.

20. A semiconductor device, comprising:

a reference potential generating circuit which operates using a power supply potential as one operational power supply potential, for generating a reference potential not dependent on said power supply potential;

an amplifying circuit receiving said reference potential from said reference potential generating circuit and a comparing potential corresponding to an internal power supply potential, for outputting a drive control signal in accordance with a potential difference between said reference potential and said comparing potential;

a drive transistor connected between a current supply node and an internal power supply potential node to which said internal power supply potential is applied, and receiving at its gate the drive control signal from said amplifying circuit; and

a current supplying circuit for supplying a current in accordance with a difference of the potential of said internal power supply potential node from a prescribed potential, to said current supply node.

21. The semiconductor device according to claim 20, wherein

said current supplying circuit includes

a current control transistor connected between a power supply potential node to which said power supply potential is applied and said current supply node, and

a current control circuit receiving said reference potential and said comparing potential for charging or discharging the gate of said current control transistor in accordance with a difference between the reference potential and the comparing potential.

23. The semiconductor device according to claim 21, wherein

said current supplying circuit further includes a start up circuit coupled to the gate of said current control transistor for setting the gate potential of said current control transistor to a predetermined potential when the power supply

potential is applied to said semiconductor device.

24. The semiconductor device according to claim 20, further comprising an internal clock signal synchronizing circuit which operates using the internal power supply potential supplied to said internal power supply potential node as one operational power supply potential, for generating an internal clock signal synchronized with an applied clock signal.

25. The semiconductor device according to claim 24, wherein

said internal clock signal synchronizing circuit includes a lock in detecting circuit for detecting lock in of said applied clock signal and said internal clock signal, and for generating a lock in signal; and

said current supplying circuit includes

a current control transistor connected between a power supply potential node to which said power supply potential is applied and said current supply node,

a current control circuit receiving said reference potential and said comparing potential for charging or discharging a gate of said current control transistor in accordance with a difference between the reference potential and the comparing potential, and

a holding circuit coupled to the gate of said current control transistor, responsive to activation of said lock in signal for holding the gate potential of said current control transistor.

28. A semiconductor device, comprising:

an analog control drive transistor coupled between a power supply potential node and an internal power supply potential node;

an analog current control circuit for comparing an internal power supply potential applied to said internal power supply potential node and a prescribed potential for controlling in analog manner a conductance of said analog control drive transistor when said internal power supply potential is lower than said prescribed potential;

a digital control drive transistor coupled between said power supply potential node and said internal power supply potential node;

a digital control circuit comparing said internal power supply potential with said prescribed potential, for rendering conductive said digital control drive transistor when said internal power supply potential is lower by a predetermined potential than said prescribed potential;

a current control transistor coupled between said power supply potential node and said digital control drive transistor; and

a current control circuit for adjusting current drivability of said current control transistor in accordance with a difference between said internal power supply potential and said prescribed potential.

29. The semiconductor device according to claim 28, wherein

said current control transistor ia a p channel MOS transistor; and

said current control circuit includes

an analog charge pump circuit for charging the gate of said current control transistor when said internal power supply potential is higher than said prescribed potential, and for discharging the gate of said current control transistor when said internal power supply potential is lower than said prescribed potential, and

a digital charge pump circuit for charging the gate of said current control

transistor when said internal power supply potential is higher by at least a predetermined voltage than said prescribed potential, and for discharging the gate of said current control transistor when said internal power supply potential is lower by at least said predetermined voltage than said prescribed potential.

30. A semiconductor device, comprising:

a first current driver transistor coupled between a power supply potential node and an internal power supply node;

a current control transistor and a second current driver transistor coupled in series between said power supply potential node and said internal power supply node in a separate path from said first current driver transistor;

a reference potential generating circuit coupled to receive a power supply potential on said power supply potential node, for generating a reference potential not dependent on fluctuation of said power supply potential, and for applying the generated reference potential to the gates of said current control transistor and said first current driver transistor;

a level shift element for level-shifting the reference potential generated from said reference potential generating circuit and outputting a level-shifted reference potential; and

a current control circuit couple to receive the internal power supply potential on said internal power supply node and the level shifted reference potential from said level shift element, for adjusting gate potential of said second current driver transistor in accordance with a difference between the level shifted reference potential and said internal power supply potential.

31. The semiconductor device according to claim 30, wherein:

said current control circuit includes a comparing circuit for comparing the internal power supply potential on said internal power supply node with said level shifted reference potential, for outputting an analog signal indicative of a result of comparison,

a digital converting circuit for converting the analog potential output from said comparing circuit to a digital potential which changes in a digital manner,

an analog charge pump circuit coupled to receive the analog signal from said comparing circuit, for adjusting the gate potential of said second current driver transistor in an analog manner in accordance with the analog signal, and

a digital charge pump circuit coupled to receive the digital potential output from said digital converting circuit for changing the gate potential of said second current driver transistor in a digital manner in accordance with the digital potential.

WEST

Generate Collection

L18: Entry 10 of 19 File: USPT Jan 19, 1993

DOCUMENT-IDENTIFIER: US 5180214 A
TITLE: Servo-type phase-locked loop anti-skid brake control system

Application Filing Date (1):
19911230

Detailed Description Text (38):
where K.sub..THETA. ' and K.sub.w ' are the control gains and which are constant. This equation tells that the servovalve input current U is proportional to both the phase error and the frequency error. In fact, this control scheme for the PLL controlled ABS is similar to the PI (proportional and integral) control algorithm with slip control. Since the wheel speed S, defined previously as S=1-Rw/V, has one-to-one correspondence to the wheel speed for a given aircraft speed. And the phase error can be regarded as the integration of frequency error, an algorithm like the PI control of the wheel speed w, or equivalently, the slip S, is actually used. The difference is only on that .THETA..sub.e is restricted to a limited range and with the modulus of 2.pi. due to the underflow and overflow characteristics of the phase detector 20.

WEST Search History

DATE: Monday, November 17, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L18	L17 and l3	19	L18
L17	(proportional$3 near2 control$4) same (integral near3 control$4) same ((pll) or (phase near lock$3 near loop$))	33	L17
L16	l15 and l3	85	L16
L15	(proportional$3 near2 control$4) and (integral near3 control$4) and ((pll) or (phase near lock$3 near loop$))	142	L15
L14	((pll) or (phase near5 frequency) near4 detect$3) same (cmos near3 invert$3) same (charge near3 pump$3)	2	L14
L13	l5 and (external$23 near2 power near2 supply$3) and l3	1	L13
L12	L11 and l9 and l8	16	L12
L11	bocure.xa. or bocure.xp.	1043	L11
L10	L9 and l7 and l8	72	L10
L9	(375/356)!.CCLS. or 375/371.ccls. or 375/354.ccls.	5188	L9
L8	(clock near3 distribut$3)	6955	L8
L7	bocure.xa. nor bocure.xp.	353518	L7
L6	L5 and l3	39	L6
L5	(clock near3 distribut$3) and ((pll) or (phase near lock$3 near loop$)) and ((phase near5 frequency) near4 detect$3) and (power near supply$3)	77	L5
L4	L3 and l2	3	L4
L3	@ad<=19970627	15284040	L3
L2	(clock near3 distribut$3) same ((pll) or (phase near5 frequency) near4 detect$3) same (power near supply$3)	18	L2
L1	(clock near3 distribut$3) same ((pll) or (phase adj2 lock$23 adj3 loop)) same (power near supply$3)	19	L1

END OF SEARCH HISTORY

WEST Search History

DATE: Monday, November 17, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L12	L11 and l9 and l8	16	L12
L11	bocure.xa. or bocure.xp.	1043	L11
L10	L9 and l7 and l8	72	L10
L9	(375/356)!.CCLS. or 375/371.ccls. or 375/354.ccls.	5188	L9
L8	(clock near3 distribut$3)	6955	L8
L7	bocure.xa. nor bocure.xp.	353518	L7
L6	L5 and l3	39	L6
L5	(clock near3 distribut$3) and ((pll) or (phase near lock$3 near loop$)) and ((phase near5 frequency) near4 detect$3) and (power near supply$3)	77	L5
L4	L3 and l2	3	L4
L3	@ad<=19970627	15284040	L3
L2	(clock near3 distribut$3) same ((pll) or (phase near5 frequency) near4 detect$3) same (power near supply$3)	18	L2
L1	(clock near3 distribut$3) same ((pll) or (phase adj2 lock$23 adj3 loop)) same (power near supply$3)	19	L1

END OF SEARCH HISTORY

L1: Entry 14 of 19 File: USPT Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6127880 A
TITLE: Active power supply filter

Brief Summary Text (7):
One aspect of maintaining a highly accurate timing signal is ensuring that the power supply to the PLL and the voltage-controlled oscillator (VCO) driving the PLL has a strictly limited amount of noise. Noise in the power supply signal to the VCO results in jitter that greatly reduces the effective frequency of the clock signal distributed over the large area of the integrated circuit. Present day and future microprocessor operating speeds are only attained if the noise in the power supply signal is highly limited.

Brief Summary Text (15):
active power supply filter are specified to best reduce power supply noise without reducing the supply current to the circuit supplied by the power supply. The active power supply filter advantageously includes a switch separating the RC filter and a target circuit that advantageously attains a high degree of noise immunity. In a phase-locked loop circuit distributing clock signals throughout an integrated circuit in a microprocessor, the active power supply filter advantageously reduces jitter so that the microprocessor executes at a higher frequency.

Detailed Description Text (33):
Referring to FIG. 6, a schematic block diagram depicts an embodiment of the PLL 402, which is included in the processor clock distribution system 400. The on-chip PLL 402 performs half-integer frequency multiplication via a divide by two frequency divider 612 in the reference bus clock (BCLK) path and performs clock generation using a circuit design that produces extremely low supply-noise-induced jitter. The PLL 402 includes a fully differential voltage-controlled oscillator (VCO) 602. The VCO 602 generates a clock signal at a clock rate that is halved by a frequency divider 606 to supply the PCLK signal at a 50% duty cycle. The PCLK signal is passed through an output multiplexer 608 to the L0/L1 global clock grid of the processor clock distribution system 400. The output multiplexer 608 selectively permits bypass of the PCLK signal and application of an alternative bypass clock signal. The PLL 402 incorporates minor-loop feedback 604 that is applied to maintain a substantially constant VCO signal amplitude independent of oscillation frequency. The minor-loop feedback 604 includes an internal replica L2/L3 clock block, a power-down replica path including the stages L2FB 418, and L3FB 420. The minor-loop feedback 604 generates the clock signal PCLK2 that is phase aligned with the clock signal PCLK. The clock signal PCLK2 is divided in clock rate by a frequency divider 610 that reduces the rate by a factor M. The reduced rate feedback clock signal is applied, along with the bus frequency divided by two by a frequency divider 612, to a phase frequency detector 620. The phase frequency detector 620 produces UP and DN pulses, each of which is translated to true and complement pulses that control a charge pump 614. The UP and DN pulses transmit phase and frequency information about the reference timing signal BCLK and the processor clock timing signal PCLK2 frequency and alignment to the charge pump 614. The phase frequency detector 620 amplifies phase detector UP and DOWN signals without distorting pulsewidth. The charge pump 614 controls the frequency of oscillation of the VCO 602 via an RC loop filter 616 which produces a loop filter voltage (LFV). The charge pump 614 uses a bandgap reference (not shown) which is based on substrate PNP transistors to produce a charge pump current that is independent of process, temperature, and power supply. The charge pump 614 has a series switch topology utilizing a voltage follower buffer (not shown) that suppresses charge sharing errors that sometimes occur when the UP and DN pulses change from the inactive mode (not controlling the LFV node) to an active mode (controlling the LFV node).

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L1: Entry 14 of 19 File: USPT Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6127880 A
TITLE: Active power supply filter

Brief Summary Text (7):
One aspect of maintaining a highly accurate timing signal is ensuring that the power supply to the PLL and the voltage-controlled oscillator (VCO) driving the PLL has a strictly limited amount of noise. Noise in the power supply signal to the VCO results in jitter that greatly reduces the effective frequency of the clock signal distributed over the large area of the integrated circuit. Present day and future microprocessor operating speeds are only attained if the noise in the power supply signal is highly limited.

Brief Summary Text (15):
active power supply filter are specified to best reduce power supply noise without reducing the supply current to the circuit supplied by the power supply. The active power supply filter advantageously includes a switch separating the RC filter and a target circuit that advantageously attains a high degree of noise immunity. In a phase-locked loop circuit distributing clock signals throughout an integrated circuit in a microprocessor, the active power supply filter advantageously reduces jitter so that the microprocessor executes at a higher frequency.

Detailed Description Text (33):
Referring to FIG. 6, a schematic block diagram depicts an embodiment of the PLL 402, which is included in the processor clock distribution system 400. The on-chip PLL 402 performs half-integer frequency multiplication via a divide by two frequency divider 612 in the reference bus clock (BCLK) path and performs clock generation using a circuit design that produces extremely low supply-noise-induced jitter. The PLL 402 includes a fully differential voltage-controlled oscillator (VCO) 602. The VCO 602 generates a clock signal at a clock rate that is halved by a frequency divider 606 to supply the PCLK signal at a 50% duty cycle. The PCLK signal is passed through an output multiplexer 608 to the L0/L1 global clock grid of the processor clock distribution system 400. The output multiplexer 608 selectively permits bypass of the PCLK signal and application of an alternative bypass clock signal. The PLL 402 incorporates minor-loop feedback 604 that is applied to maintain a substantially constant VCO signal amplitude independent of oscillation frequency. The minor-loop feedback 604 includes an internal replica L2/L3 clock block, a power-down replica path including the stages L2FB 418, and L3FB 420. The minor-loop feedback 604 generates the clock signal PCLK2 that is phase aligned with the clock signal PCLK. The clock signal PCLK2 is divided in clock rate by a frequency divider 610 that reduces the rate by a factor M. The reduced rate feedback clock signal is applied, along with the bus frequency divided by two by a frequency divider 612, to a phase frequency detector 620. The phase frequency detector 620 produces UP and DN pulses, each of which is translated to true and complement pulses that control a charge pump 614. The UP and DN pulses transmit phase and frequency information about the reference timing signal BCLK and the processor clock timing signal PCLK2 frequency and alignment to the charge pump 614. The phase frequency detector 620 amplifies phase detector UP and DOWN signals without distorting pulsewidth. The charge pump 614 controls the frequency of oscillation of the VCO 602 via an RC loop filter 616 which produces a loop filter voltage (LFV). The charge pump 614 uses a bandgap reference (not shown) which is based on substrate PNP transistors to produce a charge pump current that is independent of process, temperature, and power supply. The charge pump 614 has a series switch topology utilizing a voltage follower buffer (not shown) that suppresses charge sharing errors that sometimes occur when the UP and DN pulses change from the inactive mode (not controlling the LFV node) to an active mode (controlling the LFV node).

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L1: Entry 17 of 19 File: USPT Dec 9, 1997

DOCUMENT-IDENTIFIER: US 5696950 A
TITLE: Flexible clock and reset signal generation and distribution system having localized programmable frequency synthesizers

Abstract Text (1):
A flexible clock and reset signal generation and distribution system and method for distributing a relatively low frequency clock signal to various elements of a computer system that require higher frequency clock signals for operation and includes programmable frequency synthesizers containing phase locked loop (PLL) type frequency multipliers, which are located physically adjacent to the computer system elements for receiving the low frequency clock signal and generating the various required higher frequency clock signals. The source of the relatively low frequency clock signal is a real-time clock (RTC) module having a crystal oscillator, a reset signal generator, and a low voltage detector. The RTC module switches off the low frequency clock signal when the main system power supply falls below a prescribed voltage level, such as, a battery voltage, or a voltage reference, or a combination battery voltage and voltage reference. Further, the RTC module provides a system reset signal that is asserted a predetermined delay time after the low frequency clock signal is provided.

Brief Summary Text (14):
According to this invention, a system and method for distributing a relatively low frequency clock signal to various elements of a computer system that require higher frequency clock signals to operate, includes programmable frequency synthesizers containing phase locked loop (PLL) type frequency multipliers. These local frequency synthesizers receive the low frequency clock signal and generate the various required higher frequency clock signals. The local frequency synthesizer is positioned so that a length of the clock signal line from the local frequency synthesizer to the element is shorter than that of the clock signal line from the low frequency clock source to the local frequency synthesizer. The source of the relatively low frequency clock signal is a real-time clock (RTC) module having a crystal oscillator, a reset signal generator, and a low voltage detector. The RTC switches off the low frequency clock signal when the primary system power supply falls below a prescribed voltage level, such as, a battery voltage, or a voltage reference, or a combination battery voltage and voltage reference. Further, the RTC of the present invention provides a system reset signal that, on power-up, is asserted a predetermined delay time after the low frequency clock signal is provided.